1/4 Inch 5 Mega CMOS Image Sensor
SP5409

Specification

Version Commercial 1.2

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SuperPix Micro Technology Co., Ltd

1/4 Inch 5 Mega CMOS Image Sensor Part Number SP5409

The 1/4 inch 5-megapixel RAW data image sensor SP5409 is one of SuperPix®'s upgrade products of SP54XX series color image sensors. It is a high performance sensor based on advanced 1.4um pixel architecture. The SP5409 is a high cost-performance image sensor product that can be embedded in portable equipment, and is especially suitable for mainstream smart phones and tablet computer applications. The SP5409 incorporates 2592 x 1944 effective pixels, advanced low power analog circuits (ASP), and an improved 2-lane MIPI interface - Mobile Industry Processor Interface. The on chip ISP circuits performs sophisticated signal processing including improved black level calibration, bad pixel correction, 2x2 binning function, etc. SP5409 supports high frame speed up to 24fps at full resolution (2592 x 1944) and 30fps at 720P format (1280 x 720) transferred over a 2-lane MIPI Interface or a traditional high speed parallel interface.

Functionalities

- CMOS Image Sensor

Applications

- Mobile Phone Camera
- Tablet PC Camera
- Notebook Camera
- PC Camera
- Web Camera

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Overview

General Description

SuperPix® SP5409 is a low-cost, high performance 1/4 inch 5 Mega pixels image sensor, which is the latest production derived from SuperPix® the 2nd generation CMOS image sensor technology. It is loaded with sophisticated features such as advanced 1.4um pixel structure which is a significant breakthrough on the cutting edge of domestic pixel technology and plenty of new functions. The SP5409 is based on the 1.4um x 1.4um CMOS image sensor pixel architecture by proprietary design of SuperPix®, making it an ideal choice for high-end and mainstream smart phone. Further more, the embedded two lanes MIPI interface enables rapid data transfer, increasing reliability, reducing power consumption and also eliminating facility compatibility issues.

In order to Extend SuperPix®'s strategy of high quality and high-end sensor for smart phone market and relative portable equipments , several efficient features enables the SP5409 to achieve best-in-class 5 Mega images and videos. For instants, the advanced 1.4um pixel architecture is able to increased sensitivity per unit area, improved quantum efficiency, and reduced crosstalk. With perfect low-light performance, SP5409 enables a new generation of high-performance camera phone that deliver top quality digital photographs.

All though SP5409 is a RAW sensor, it includes a variety of image control functions, for instance, upgraded black level calibration, refined bad pixel correction, 2 x 2 binning function, and so forth, all of which lead to significant improvement in image quality, even in the most challenging lighting conditions. Moreover, SP5409 supports high frame speed up to 24fps at 2592 x 1944 (5 Mega, QSXGA) resolution and 30fps at 1280 x 720 (0.9 Mega, 720P) resolution transferred over the 2-lane MIPI interface, which can deliver the high image quality to users swiftly. These prominent features integrated in SP5409 will result in vivid still and video images, and make it an effective solution for ultra-slim camera designs for next-generation mobile handsets, smart phones and tablets.

An overview of the SP5409 Image Sensor features and functions will be given below.

Function Diagram

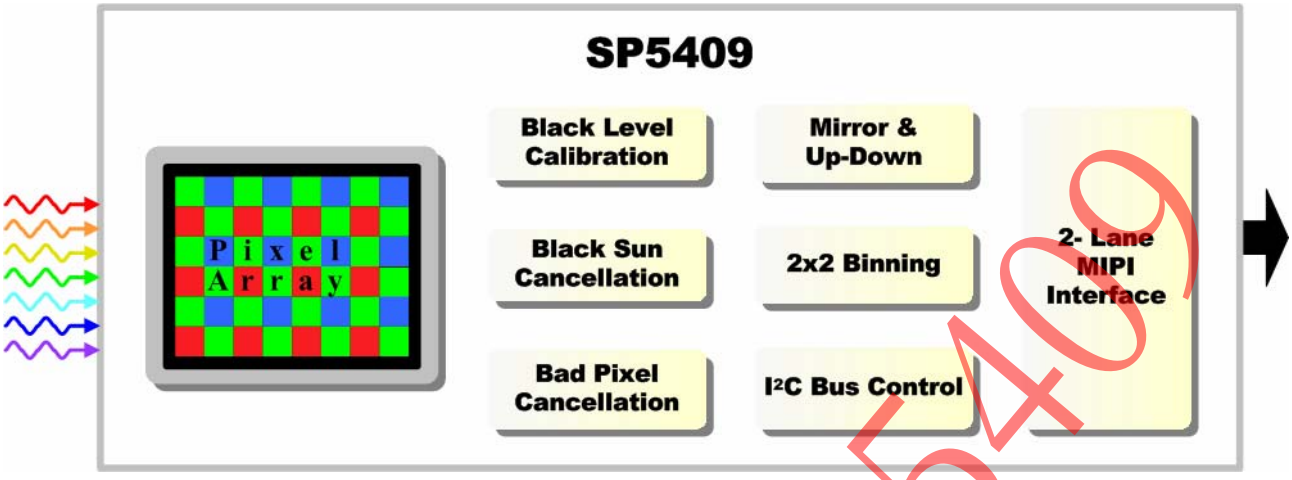


Figure 1 Function Diagram

Typical Application List

- Mobile Phone Camera
- Tablet PC Camera
- Notebook Camera
- PC Camera
- Web Camera

Typical Application Diagram

Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	2592 x 1944
Pixel Size	1.4um x 1.4um Square Pixel
Lens Size	1/4 inch
Color Filter	Primary Color Filter Bayer arrangement
Power Supply	I/O 1.7V ~ 3.0V
	DVDD18 1.7V ~ 3.0V
	Analog 2.6V ~ 3.0V
Power consumption	Active TBD
	Standby TBD
Data format	Raw8
	Raw10
Output Formats	CSI-2 2lanes
Input Clock	10 – 30 MHz
Max. Frame Rate	24fps@2592 x 1944 Mode
	30fps@1920 x 1080 Mode
	30fps@1296 x 972 Mode
	30fps@1280 x 720 Mode
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	COB / TSV

Table 1 Key Performance Parameters

Features List

- Support QSXGA (5Mega 2592x1944) resolution
- Support 1080P (2Mega, 1920x1080) resolution
- Support 720P (0.9Mega, 1280x720) resolution
- Advanced 1.4um x 1.4um pixel architecture
- Support night mode
- Support mirror and up-down function
- Support embedded black level calibration
- Support bad pixel cancellation
- Support black sun cancellation
- Support 8bit and 10bit raw image data output
- Support I²C bus controlling registers inside chip
- Support 2x2 binning function
- Support 2-lane MIPI interface
- Support mainstream mobile phone platforms

Function Description

Pixel Array Structure

The SP5409 pixel array is configured as of 2628 columns by 2008 rows, and the effective array size is 2592 x 1944, while the active array size is 2612 x 1960. The details of pixel array are shown below.

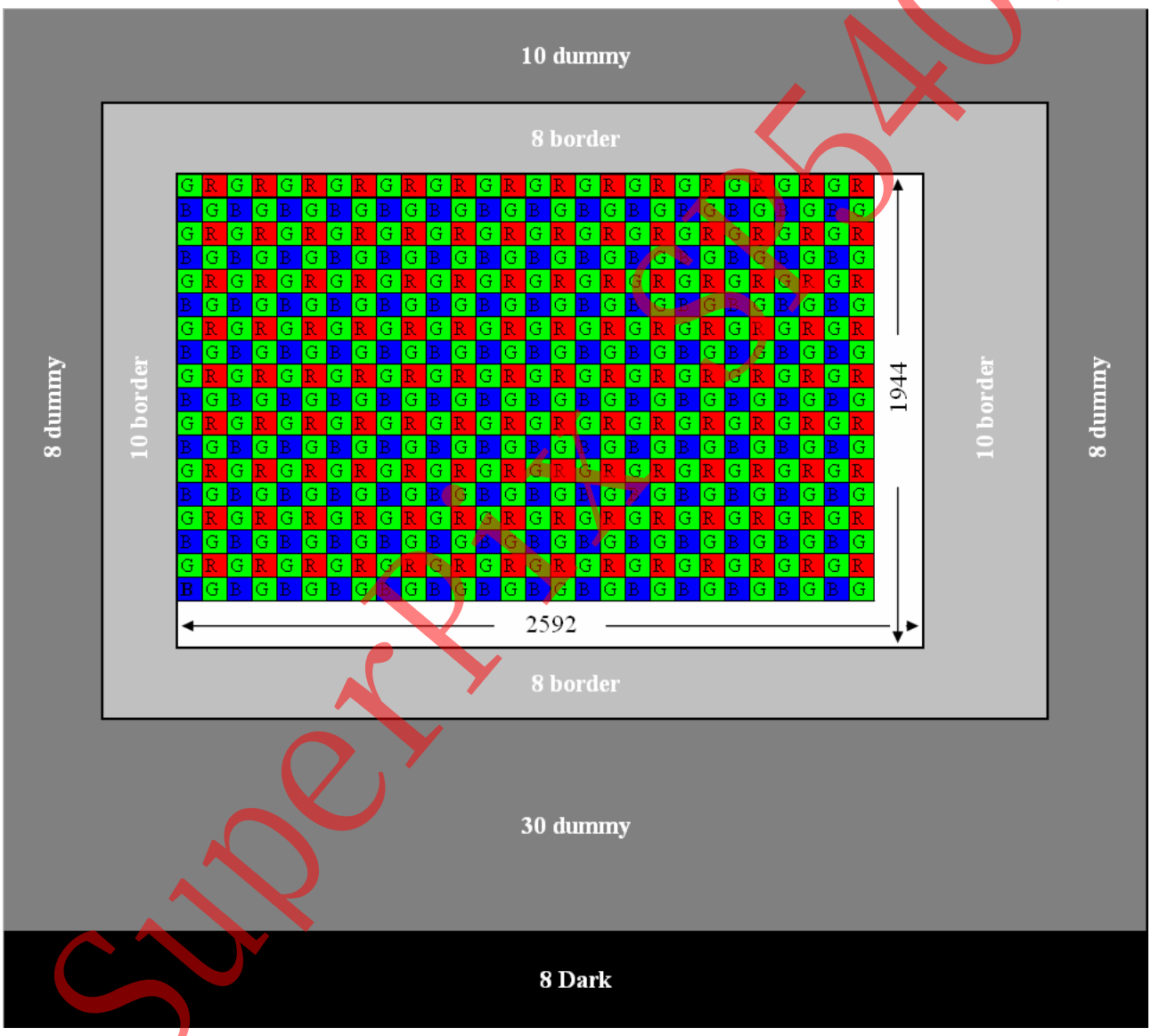


Figure 3 Pixel Floor Plan

Note：
The color filter of the first pixel at left bottom is blue.

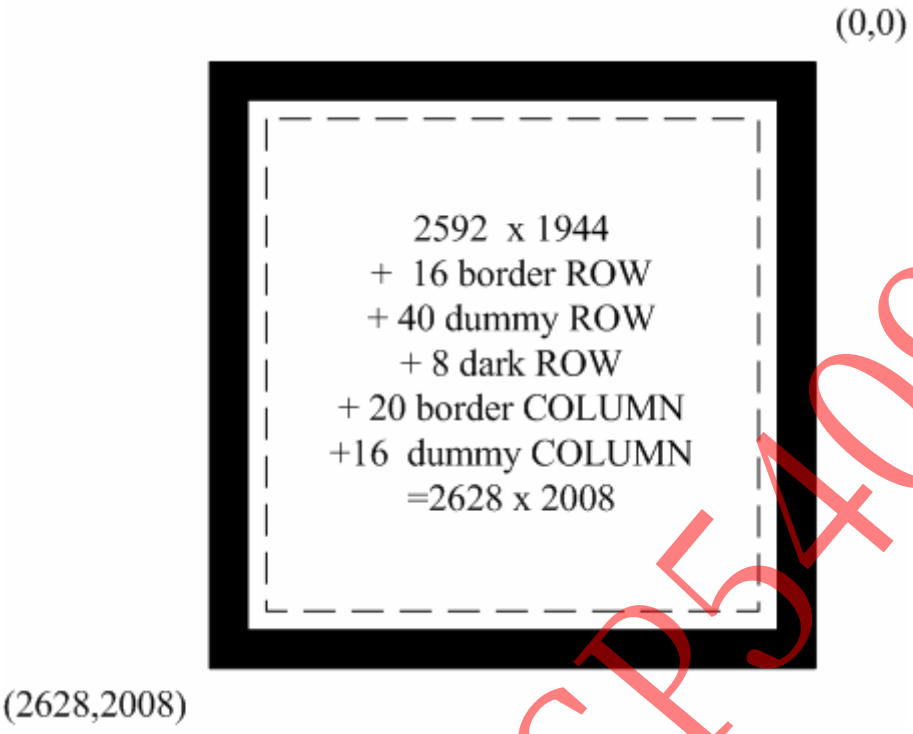


Figure 4 Sensor Pixel Description

Sensor Image Signal Processor Functionality

- Mirror and Up-Down
- Windowing
- Test Pattern
- Automatic Black Level Calibration
- Bad Pixel Correction

Mirror and UP-Down

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.

Original **Mirrored** **Up-Down** **Mirrored and Up-Down**

Windowing

The embedded windowing function extract an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By property setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Auto Black Level Calibration

The pixel array contains several optically black lines, which can be seen at the pixel array structure section. These lines are used to provide the data for black level calibration and further correction.
When the strobe signal is triggered in mode 2, the strobe signal will be launched immediately, and the next frame – the one is colored shown at the figure above – then

can be exposed accurately.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit.

A bad pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

Output Interface

MIPI Serial Interface

MIPI Serial Interface – Mobile Industry Processor Interface is the most important data transport path for the next generation mobile phone, which defines standards for the interface between SP5409 modules of a mobile. The MIPI interface can support large data stream better than any other data interface. With it the sensor can provide more high definition images to the mobile phone. More over, the MIPI interface enables rapid data transfer, increasing reliability, reducing power consumption and also eliminating facility compatibility issues.

MIPI interface provides one single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Data lane has full support for HS (uni-directional) and LP (bi-directional) data transfer mode.

PLL and Clock Generator

The sensor contains a Phase Locked Loop (PLL) block, which generates all the necessary internal clocks from the external clock input.

Address	Register Name	Bits	Description	Default
P0:0x2f	pll_ctrl_buf	7~0	[6:2] pll_nc [1:0] pll_mc	0x24
P0:0x30	clk_mode_buf	7~0	[6]pll_clk_sel 0:select pll output 1:select external clock [3:2]clk_cp_crtl 00---clk_cp = 1/2pll_clk 01---clk_cp = 1/4 pll_clk 10---clk_cp = 1/6 pll_clk 11---clk_cp = input clk [1~0]ISP clock setting (by pclk) 00---dclk = - 1/2 pll_clk 01---dclk = 1/4 pll_clk 10---dclk = 1/8 pll_clk 11---dclk = - 1/16 pll_clk	0x15
P0:0x33	dac_clk_mode_buf, cis_clk_mode_buf	3~0	[3:2]Dac_clk_mode_buf 00--- dac_clk = 1/2pll_clk 01--- dac_clk = 1/4 pll_clk 10--- dac_clk = 1/6 pll_clk 11--- dac_clk = 1/8 pll_clk [1:0] cis_clk_mode_buf 00--- timer_clk = 1/2pll_clk 01--- timer_clk = 1/4 pll_clk 10--- timer_clk = 1/8 pll_clk 11--- timer_clk = 1/16 pll_clk	0x09

I²C Bus

Single READ and Single WRITE

The SP5409 I²C write address and read address can be chosen by I²C ID pad. When the pad is set high, the write address is 0x7A and the read address is 0x7B, while the pad is set low, the write address is 0x78 and the read address is 0x79.

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

The figure shown below will illustrate SP5409 single READ sequence and single WRITE sequence.

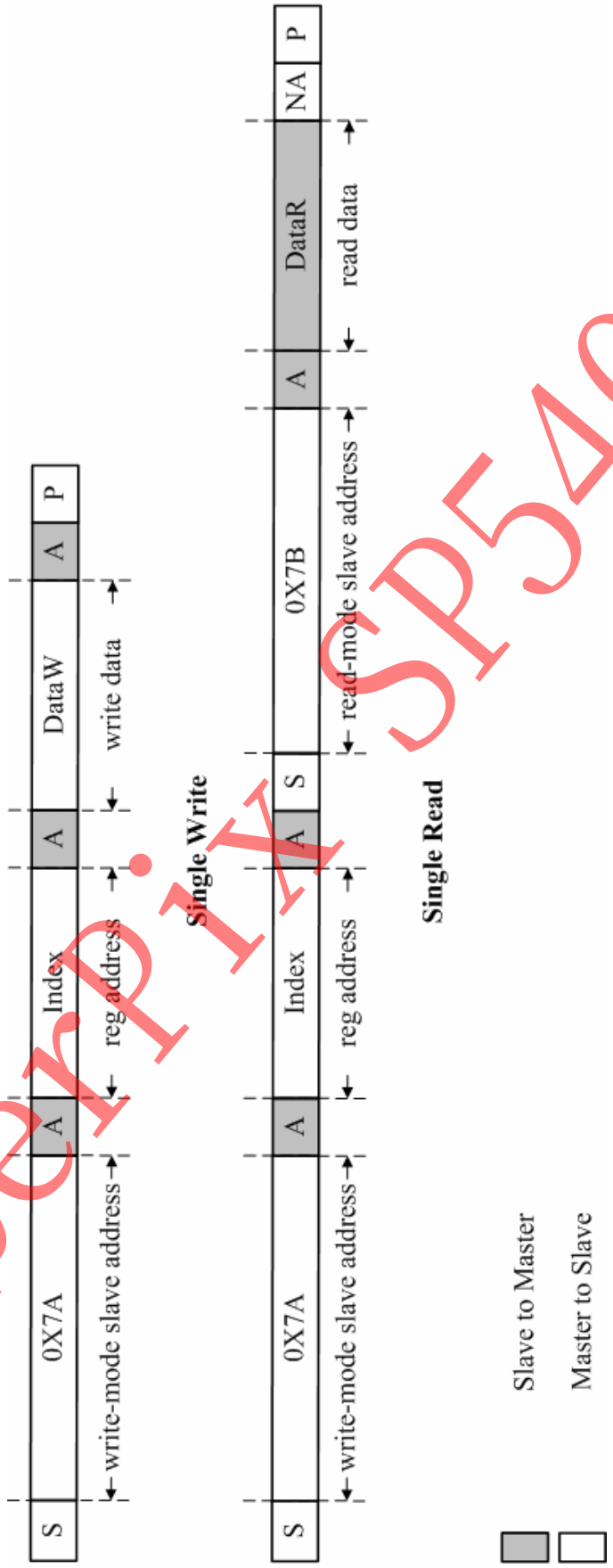


Figure 5 I²C Read & Write Message Description – I²C ID PAD set high

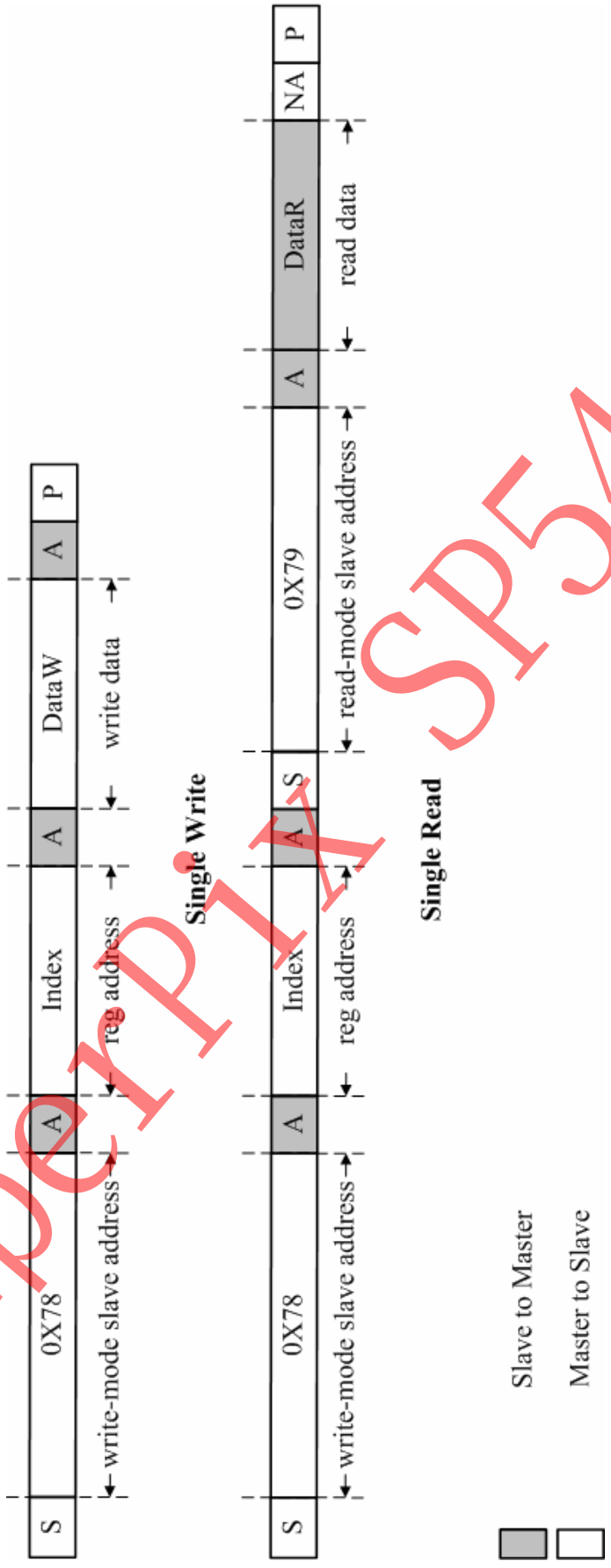


Figure 6 I²C Read & Write Message Description – I²C ID PAD set low

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP5409 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

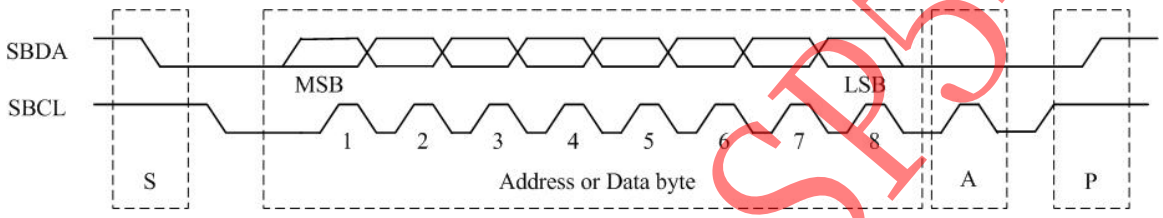


Figure 7 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

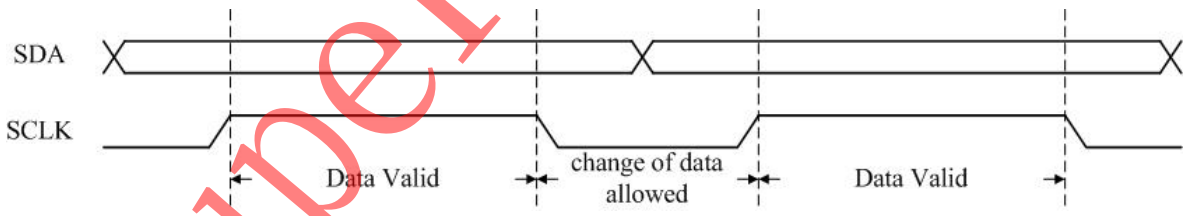


Figure 8 I²C Data Transport Description

Timing Parameter

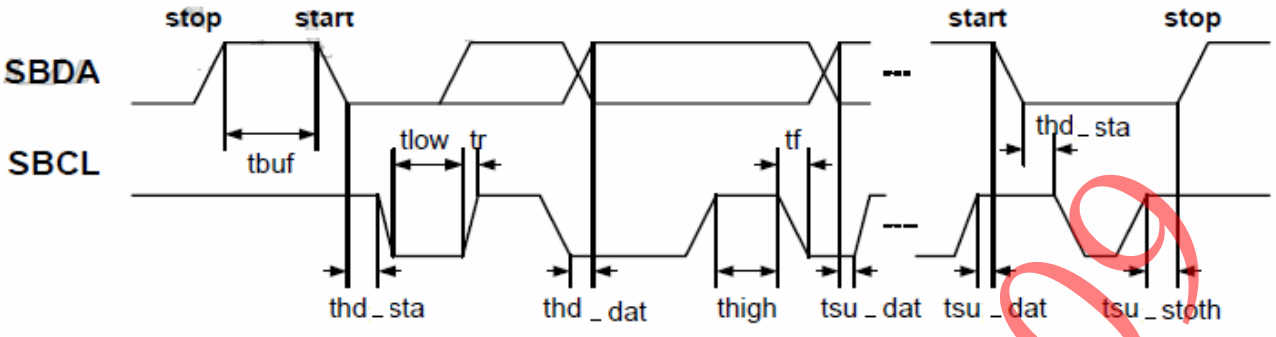


Figure 9 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

DC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.6	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		0.3xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			0.3xVDDIO	V
T	Junction Temperature	-20	25	70	**℃**

Absolute Maximum Ratings

Supply Voltage (with respect to Ground)	AVDD	4.5V
	DVDD	3V
	DVDDIO	4.5V
All Input/Output Voltages (with respect to Ground)	-0.3V to DVDDIO+1V	
Ambient Storage Temperature	High	150°C 1000hrs
	Low	-40°C 168hrs
Peak solder temperature (10 second dwell time)	260℃	
Electro Static Discharge (ESD)	2000V	

Note:

Exceeding the absolute maximum rating shown above can invalidate all AC and DC electrical specifications and may result in permanent device

Power Up/Off Sequence

Power Up Sequence

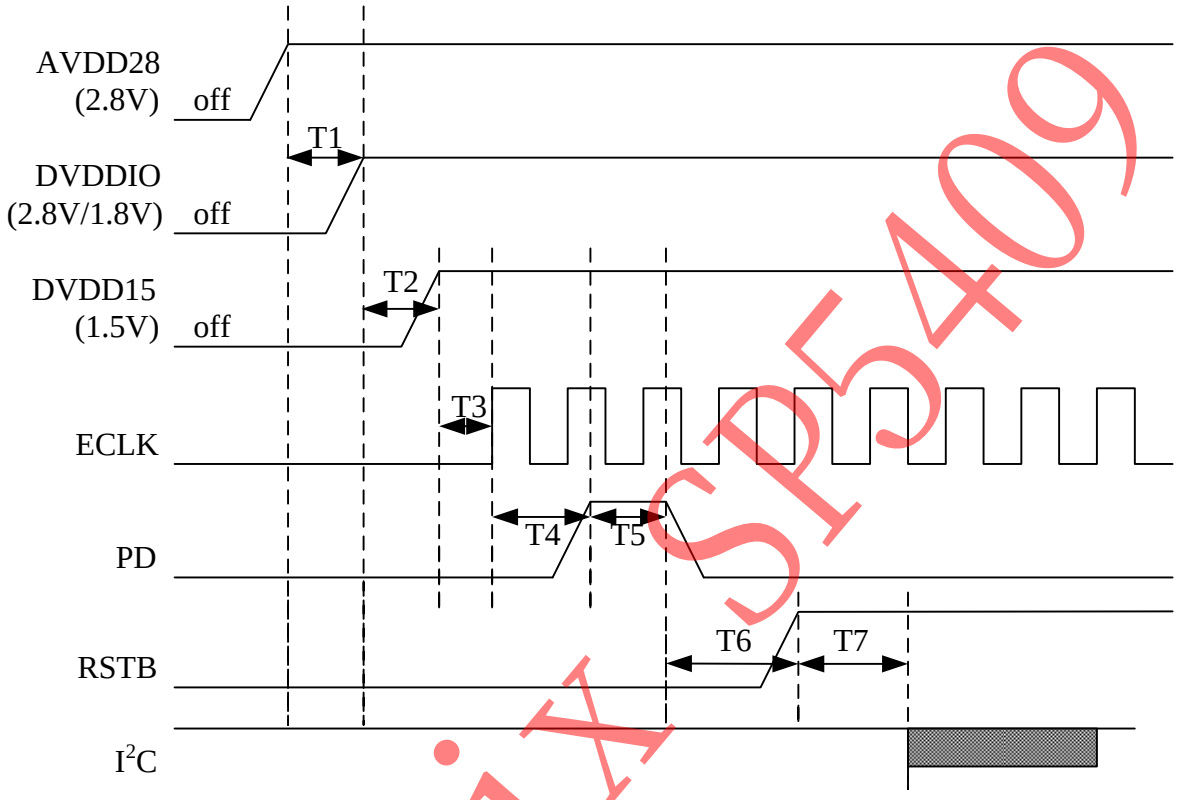


Figure 10 Power Up Sequence

Symbol	Description	Min	Unit
T1	Time from AVDD28 to DVDDIO	0	ms
T2	Time from DVDDIO to DVDD15	0	ms
T3	Time from DVDD18 to clock plus input	0	ms
T4	Time from ECLK to PD up edge	0	ms
T5	PD high plus time	100	ns
T6	Time from PD dn edge to RSTB up edge	0	ms
T7	Time from RSTB up edge to available I2C	5	ms

Note:

1. The SP5409 sensor includes a RSTB pin that forces a complete hardware reset when it is pulled low(GND). The SP5409 sensor also includes POR circuit which generate reset signal when power up.

2. POR generates the reset signal only occurs at power up, but RSTB generates the reset signal at anytime.

3. If necessary, the SP5409 could used the RSTB to generate the hardware reset that following above timing. If not, the RSTB should be connect DVDDIO.

Power Off Sequence

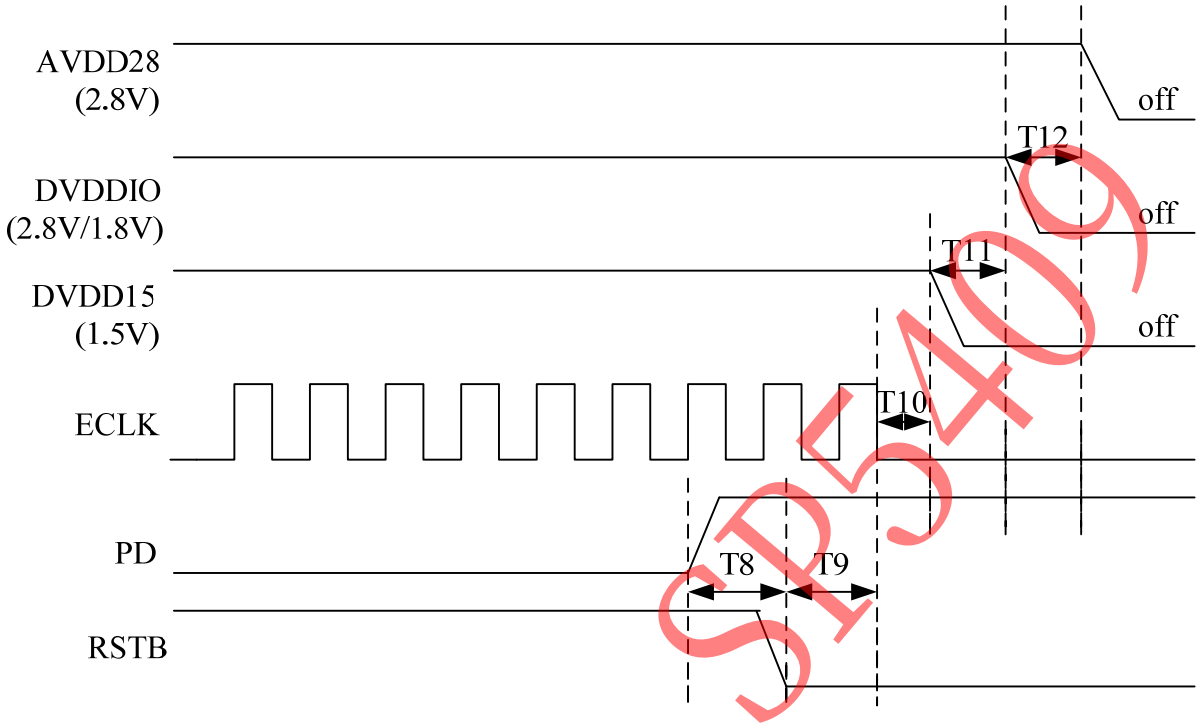


Figure 11 Power Off Sequence

Symbol	Description	Min	Unit
T8	Time from PD up edge to RSTB dn edge	0	ms
T9	Time from RSTB dn edge to ECLK	0	ms
T10	Time from ECLK to DVDD15	0	ms
T11	Time from DVDD18 to DVDDIO power down	0	ms
T12	Time from DVDDIO to AVDD28 power down	0	ms

Note:

1. If necessary, the SP5409M could used the RSTB to generate the hardware reset that following above timing. If not, the RSTB should be connect DVDDIO.

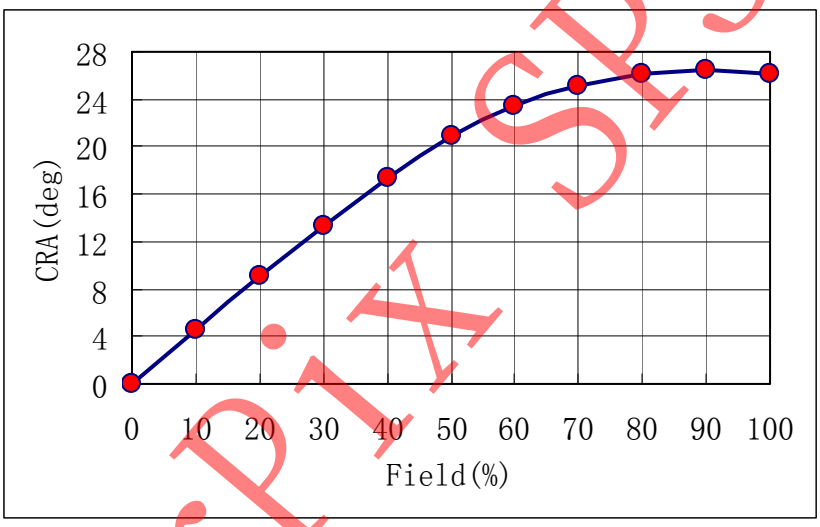
CRA Information

Pixel Array Information

Unit Pixel Size: 1.4um

		Value
Active pixel array	X-axis	2592
	Y-axis	1944
RIC(mm)	X-axis edge	1.814
	Y-axis edge	1.361
	Diagonal edge	2.268

RIC: Radius from the Image Center

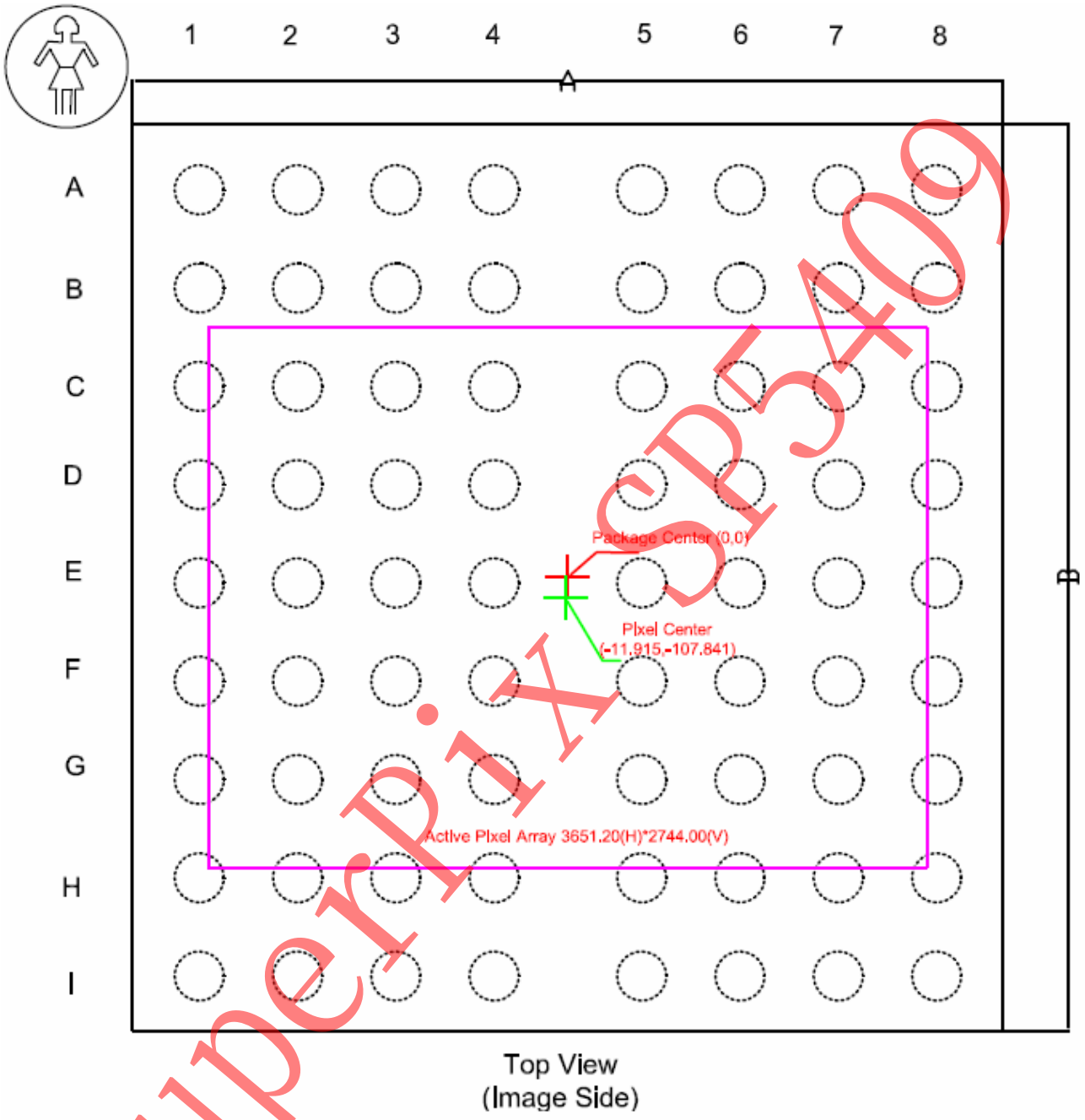


Field(%)	RIC(mm)	CRA(deg)
0	0	0
10	0.2268	4.6
20	0.4536	9.1
30	0.6804	13.4
40	0.9072	17.4
50	1.134	20.9
60	1.3608	23.4
70	1.5876	25.1
80	1.8144	26.2
90	2.0412	26.4
100	2.268	26.1

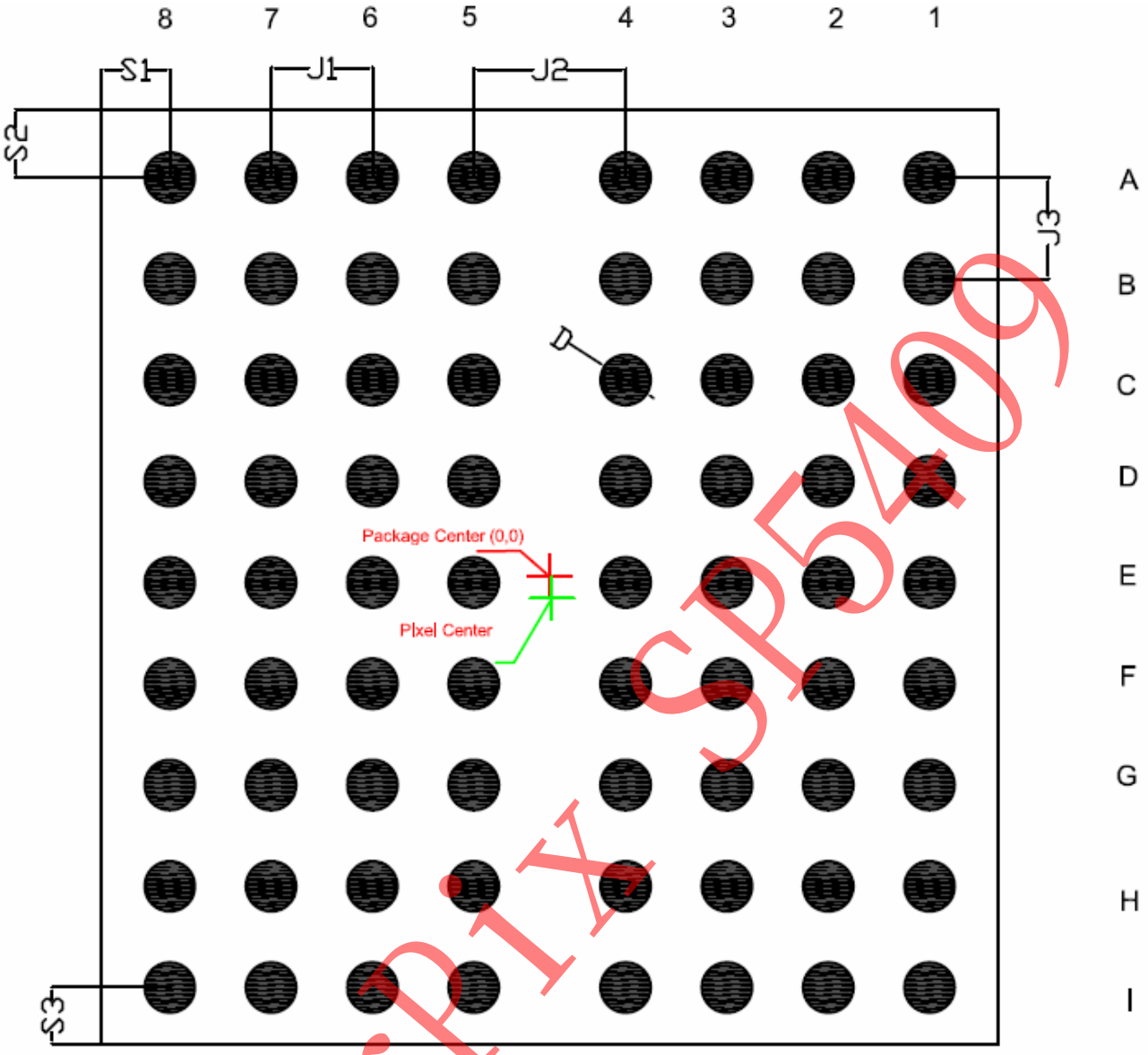
Figure 12 CRA Information

Package Information

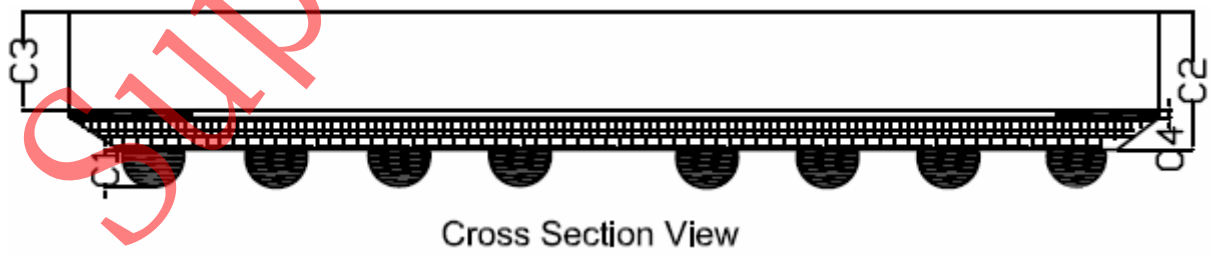
Unit: um



Top View
(Image Side)



Bottom View
(BGA Side)



Cross Section View

Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	4426	4401	4451
Package Body Dimension Y	B	4617	4592	4642
Package Height	C	679	610	748
Ball Height	C1	152	90	214
Package Body Thickness	C2	527	459	595
Glass Thickness	C3	375	340	410
Cavlty Wall Thlckness	C4	40	30	50
Ball Diameter(before reflow)	D	250	220	280
Total Pin count	N	72	-	-
Pin count X axls	N1	8	-	-
Pin count Y axls	N2	9	-	-
Pin pitch X axls1	J1	500	490	510
Pin pitch X axls2	J2	750	740	730
Pln pltch Y axls1	J3	500	490	510
BGA ball center to package center offset in X direction	X	0	-0.025	0.025
BGA ball center to package center offset in Y direction	Y	-30.116	-55.000	-5.000
Edge to Ball Center Distance along X axls	S1	338	308	368
	S2	338	308	368
Edge2 to Ball Center Distance along Y axls	S3	338.6	309	369
	S4	278.4	248	308

Table 2 Package Dimension

	1	2	3	4	5	6	7	8
A	MVDD18	OUTCN	OUTDN0	OUTDN1	DVDD15	DVDD15	DVDD15	DVDD15
B	MGND	OUTCP	OUTDP0	OUTDP1	DGND	DVDD18	DVDD18	DGND
C	DVDD28	MVDD15	MVDD15	MVDD15	DGND	DVDD18	ECLK	PD
D	AGND28	DGND	DGND	DGND	DGND	BYPASS	SBDA	D0
E	AGND28	DVDD28	DVDD28	DVDD28	DVDD28	DVDD28	DVDD28	SBCL
F	AGND28	AVDD28	AVDD28	AVDD28	AVDD28	AVDD28	I2CID	RST
G	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28
H	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28	AGND28
I	TEST	AVDD28	AVDD28	AVDD28	AVDD28	AVDD28	AVDD28	AGND28

Table 3 Ball Name

PIN No.	PIN Name	I/O	Description
A1	MVDD18	MP	MIPI Power 1.8V
A2	OUTCN	O	MIPI clock output -
A3	OUTDN0	O	MIPI data0 output -
A4	OUTDN1	O	MIPI data1 output-
A5	DVDD15	DP	While "BYPASS" Pin connect to"0",internal power supply 1.5V. While "BYPASS" Pin connect to"1",external power supply 1.5V.
A6	DVDD15	DP	While "BYPASS" Pin connect to"0",internal power supply 1.5V. While "BYPASS" Pin connect to"1",external power supply 1.5V.
A7	DVDD15	DP	While "BYPASS" Pin connect to"0",internal power supply 1.5V. While "BYPASS" Pin connect to"1",external power supply 1.5V.
A8	DVDD15	DP	While "BYPASS" Pin connect to"0",internal power supply 1.5V. While "BYPASS" Pin connect to"1",external power supply 1.5V.
B1	MGND	MG	MIPI Ground
B2	OUTCP	O	MIPI clock output+
B3	OUTDP0	O	MIPI data0 output+
B4	OUTDP1	O	MIPI data1 output+
B5	DGND	DG	Digital Ground
B6	DVDD18	DP	Digital Power1.8V
B7	DVDD18	DP	Digital Power1.8V
B8	DGND	DG	Digital Ground
C1	DVDD28	DP	Digital Power2.8V
C2	MVDD15	MP	External Connect capacitance(1uF)
C3	MVDD15	MP	External Connect capacitance(1uF)
C4	MVDD15	MP	External Connect capacitance(1uF)
C5	DGND	DG	Digital Ground
C6	DVDD18	DP	Digital Power1.8V
C7	ECLK	I	Input Clock
C8	PD	I	PWDN Control, "0" normal
D1	AGND28	AG	Analog Ground
D2	DGND	DG	Digital Ground
D3	DGND	DG	Digital Ground
D4	DGND	DG	Digital Ground
D5	DGND	DG	Digital Ground
D6	BYPASS	I	"0"Internal Power supply,"1"External Power supply.
D7	SBDA	I/0	Slave Tri-state,I2C data bus
D8	D0	I/0	Multiplexing Pad for sync mode or test mode
E1	AGND28	AG	Analog Ground
E2	DVDD28	DP	Digital Power2.8V
E3	DVDD28	DP	Digital Power2.8V
E4	DVDD28	DP	Digital Power2.8V
E5	DVDD28	DP	Digital Power2.8V

E6	DVDD28	DP	Digital Power2.8V
E7	DVDD28	DP	Digital Power2.8V
E8	SBCL	I	Slave I2C clock bus
F1	AGND28	AG	Analog Ground
F2	AVDD28	AP	Analog Power2.8V
F3	AVDD28	AP	Analog Power2.8V
F4	AVDD28	AP	Analog Power2.8V
F5	AVDD28	AP	Analog Power2.8V
F6	AVDD28	AP	Analog Power2.8V
F7	I2CID	I	Device Address
F8	RST	I	Reset Signal,Low level reset
G1	AGND28	AG	Analog Ground
G2	AGND28	AG	Analog Ground
G3	AGND28	AG	Analog Ground
G4	AGND28	AG	Analog Ground
G5	AGND28	AG	Analog Ground
G6	AGND28	AG	Analog Ground
G7	AGND28	AG	Analog Ground
G8	AGND28	AG	Analog Ground
H1	AGND28	AG	Analog Ground
H2	AGND28	AG	Analog Ground
H3	AGND28	AG	Analog Ground
H4	AGND28	AG	Analog Ground
H5	AGND28	AG	Analog Ground
H6	AGND28	AG	Analog Ground
H7	AGND28	AG	Analog Ground
H8	AGND28	AG	Analog Ground
I1	TEST	O	Test pin
I2	AVDD28	AP	Analog Power2.8V
I3	AVDD28	AP	Analog Power2.8V
I4	AVDD28	AP	Analog Power2.8V
I5	AVDD28	AP	Analog Power2.8V
I6	AVDD28	AP	Analog Power2.8V
I7	AVDD28	AP	Analog Power2.8V
I8	AGND28	AG	Analog Ground

Table 4 Pin Description

Registers

System Register

Address	Register name	Bits	Description	Default
P0:0x02	chip_id	7~0	chip_id (read only)	0x54
P0:0x03	chip_id	7~0	chip_id (read only)	0x09
P0:0x2f	pll_ctrl_buf	7~0	[6:2] pll_nc [1:0] pll_mc	0x24
P0:0x30	clk_mode_buf	7~0	[6]pll_clk_sel 0:select pll output 1:select external clock [3:2]clk_cp_crtl 00---clk_cp = 1/2pll_clk 01---clk_cp = 1/4 pll_clk 10---clk_cp = 1/6 pll_clk 11---clk_cp = input clk [1~0]ISP clock setting (by pclk) 00---dclk = - 1/2 pll_clk 01---dclk = 1/4 pll_clk 10---dclk = 1/8 pll_clk 11---dclk = - 1/16 pll_clk	0x15
P0:0x33	dac_clk_mode_buf, cis_clk_mode_buf	3~0	[3:2]Dac_clk_mode_buf 00--- dac_clk = 1/2pll_clk 01--- dac_clk = 1/4 pll_clk 10--- dac_clk = 1/6 pll_clk 11--- dac_clk = 1/8 pll_clk [1:0] cis_clk_mode_buf 00--- timer_clk = 1/2pll_clk 01--- timer_clk = 1/4 pll_clk 10--- timer_clk = 1/8 pll_clk 11--- timer_clk = 1/16 pll_clk	0x09
P0:0x34	buf_pll_outdiv	1~0	Pll frequency divider control 00--- 1 01--- 2 10--- 4 11--- 8	0x00

Sensor Register

Address	Register name	Bits	Description	Default

P1:0x03	buf_exp_8msb	7~0	Integration time high 8 bits	0x01
P1:0x04	buf_exp_8lsb	7~0	Integration time low 8 bits	0x20
P1:0x05	vblank_buf_8msb	7~0	Vertical blank high 8 bits	0x00
P1:0x06	vblank_buf_8lsb	7~0	Vertical blank low 8 bits	0x00
P1:0x09	hblank_4msb	3~0	Horizontal blank high 4 bits	0x00
P1:0x0a	hblank_8lsb	7~0	Horizontal blank low 8 bits	0x00
P1:0x0d	test_en	0	Test Pattern test enable 1: enable 0: disable	0x00
P1:0x18	rst_del_en, rst_colrow_en	4~0	Sensor column and row reset control [4] rst_del_en When enabled, the sensor will delete the first synchronized frame 1: enable 0: disable [0] rst_colrow_en 1: enable 0: disable	0x00
P1:0x23	Rpc	7~0	PGA Gain control(1X~15.5X)	read only
P1:0x31	buf_comm_ctrl	7~0	Sensor resolution mode selection [7]ana_v_window_mode [6]reserved [5]bypass_dsp [4]mode_iris [3]subsample [2]2x2 binning [1]1080p [0]720p	0x00
P1:0xa1	tx_speed_area_sel	2~0	MIPI transmission speed select	0x03
P1:0xa2	r_init_m	7~0	MIPI initial time control bit 15~8	0x27
P1:0xa3	r_init_l	7~0	MIPI initial time control bit 7~0	0x10
P1:0xa4	mipi_en_buf, r_exit, r_wakeup_mh	6~0	[6] mipi_en_buf, Mipi enable [5:2] r_exit, Data lane exit time control [1:0]MIPI wakeup time control bit 17~16	0x2d
P1:0xa5	r_wakeup_m	7~0	MIPI wakeup time control bit 15 ~8	0x86
P1:0xa6	r_wakeup_l	7~0	MIPI wakeup time control bit 7 ~0	0xa0
P1:0xae	frame_end_dly[7:0]	7~0	Frame end delay control	0x65
P1:0xaf	frame_end_dly[15:8]	7~0	Frame end delay control	0x00
P1:0xb1	shutdowna	0	Mipi phy shutdown	0x00
P1:0xb3	pwd_mipi	0	Mipi ldo powerdown	0x01
P1:0xc1	mipi_pll_nc,	6~0	[6:2] mipi_pll_nc, MIPI pll nc control	0x09

	mipi_pll_mc		[1:0] mipi_pll_mc , MIPI pll mc control	
P1:0xc4	mipi_pll_sel, mipi_pll_en, mipi_pll_outdiv, mipi_pll_outen_delay	6~0	[6] mipi_pll_sel [5] mipi_pll_en [4:3] mipi_pll_outdiv [2:0]MIPI pll output delay control	0x48

ISP Register

Address	Register name	Bits	Description	Default
P2:0x35	buf_outmode1	5~0	[5] unpro_raw_out_en	0x00
P2:0x36	buf_outmode2	4~0	[4] domu_en [3] VSYNC Inversion [2] HSYNC Inversion [1] Disable HSYNC & VSYNC	0x00
P2:0xa0	dem_v_start_3msb[2:0]	2~0	Image vertical start 3msb	0x00
P2:0xa1	dem_v_start_8lsb	7~0	Image vertical start 8lsb	0x00
P2:0xa2	dem_v_size_3msb[2:0]	2~0	Image vertical size 3msb	0x07
P2:0xa3	dem_v_size_8lsb	7~0	Image vertical size 8lsb	0xa8
P2:0xa4	dem_h_start_3msb[2:0]	2~0	Image horizontal start 3msb	0x00
P2:0xa5	dem_h_start_8lsb	7~0	Image horizontal start 8lsb	0x00
P2:0xa6	dem_h_size_3msb[2:0]	2~0	Image half horizontal size 3msb	0x05
P2:0xa7	dem_h_size_8lsb	7~0	Image half horizontal size 8lsb	0x18

Page Selection

Address	Register name	Bits	Description	Default
0xfd	page_flg_d2	3~0	[2:0] page select 000---page0 001---page1 010---page2	0x00

Revision History

Version #	Date	Modification
Commercial 1.0	2014.05.27	1. The first release for customers. 2. Pixel information, I^2C information, Power UP / OFF, CRA information has been confirmed 3. Package information has not been confirmed.
Commercial 1.1	2014.07.04	1. add registers description 2. add package information
Commercial 1.2	2014.07.08	1. update package information