DATA SHEET

IT03A1

- Resolution: 648x488 VGA
- Optical Size (CRA): 1/10″ (25.6)
- Rev: 00 (2015.03.09)

Image Tech

- Contents -

1. General information of IT031A1

1.1 Overview

IT03A1 is a CMOS Image Sensor SOC chip for the application as described in section "1.3" below;. It has 648x488 valuable resolution with 1/10" optical format and low dark noise, high sensitivity and very low power imaging system. All required image processing function such as auto exposure control, auto white balance control, lens shading correction, auto defect correction reducing FPN (Fixed Pattern Noise), H/V line noise, random noise and so on, are programmable through the two wire bus communication system.

1.2 Features

- 2.115um x 2.115um pixel
- resolution : 640H x 480V
- max. frame rate : 30fps @ VGA
- image size : VGA and programmable windowing
- support for output formats : YUV422, RAW bayer
- image flip : horizontal / vertical mirror
- two-wire serial bus control
- image signal processing : auto exposure, auto white balance, dead pixel correction, edge enhancement, color correction and etc.

1.3 Application in industry

- Cellular Phone Cameras
- Notebook, PC, Tablet cameras
- PDAs, Toys, Wearables
- Digital still cameras and camcorders
- IPVS (Internet Protocol Video System)
- Black Box in car, CCTV for Security/Environment systems
- Medical equipment

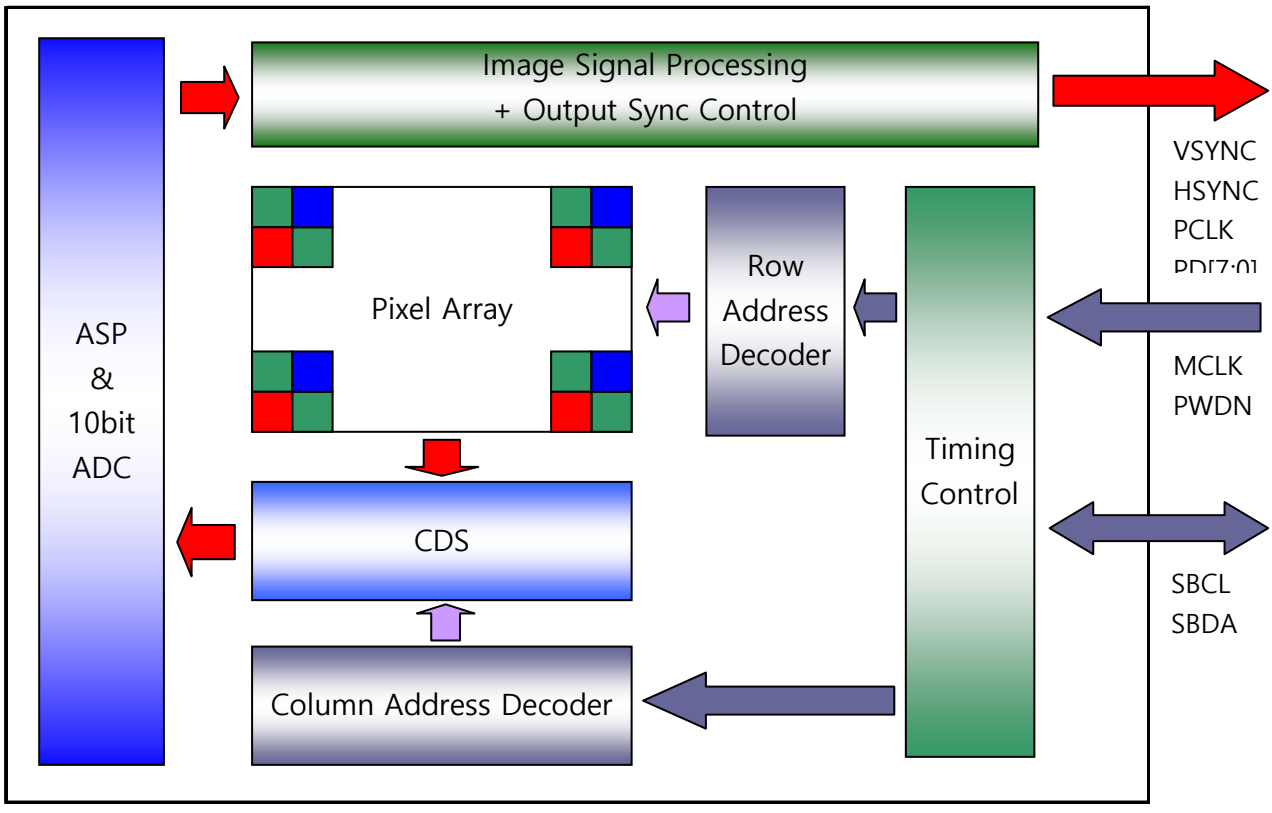
1.4 Technical Specifications

[Table-01]

Parameter	Description
Optical Format	1/10 inch
Active Pixel Array	648 x 488
Pixel Size	2.115um x 2.115um
Max Frame Rate	VGA 30fps @ 24MHz
Optimal lens chief ray angle	25.6° (Linear)
ADC Resolution	10 bits
Power Supply	VDDIO : 1.8 ~ 2.8V norminal
	AVDD : 2.8V norminal
Power Consumption	TBD mW @ 30fps VGA
	,TBD uA @ standby
max SNR(S/N Ratio)	TBD
Dark Current	TBD
Sensitivity	TBD
Operating Temperature	TBD
Stable Image Temperature	TBD
Dynamic Range	TBD

1-5. Block diagram

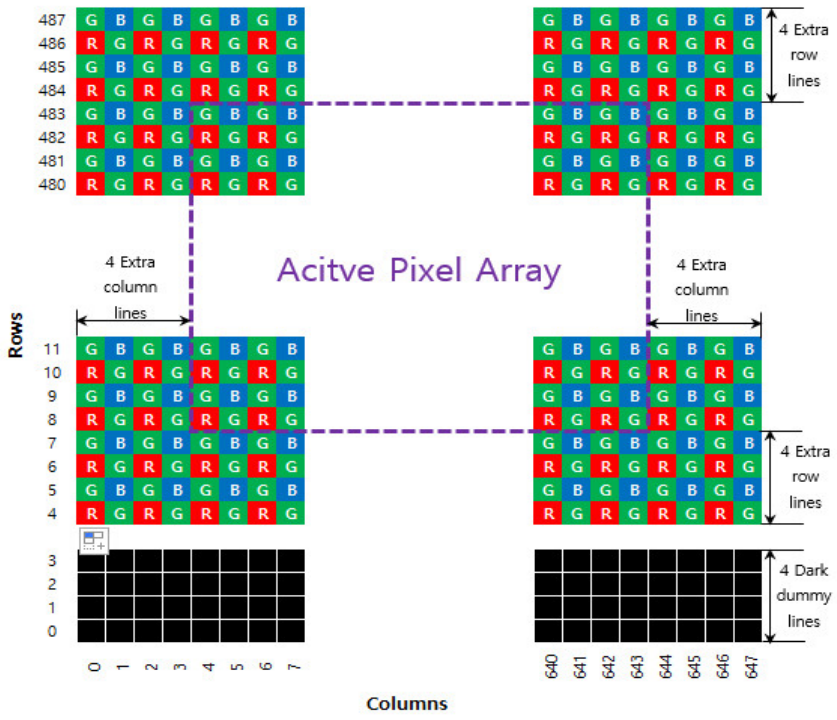
[Figure-01] Block Diagram



IT03A1 is a CMOS active pixel type image sensor. Figure-01 shows the functional block diagram of the IT03A1. It is embedded with active imaging pixel array, row/column driver circuit, CDS circuit to reduce fixed pattern noise, analog amplifier to control global gain under different light condition, ASP to process the analog signal, 10bit A/D converter which transfers the analog signal to digital signal, ISP to process the digital signal, timing control circuit for imaging scanning and frame rate, and two-wire serial bus to control these functions,

1.6 Pixel Array

The IT03A1 sensor is configured as 648 columns by 488 rows. Extra pixels and dark row pixels are added outside the active pixel array. Figure-01 shows a cross-section of the image sensor array. Pixel array is covered by Bayer pattern color filters. The primary color RG/GB array is arranged in line-alternating way. Since each pixel can have only one type of color filter on It, only one color component can be obtained by a pixel. IT03A1 can provide the Raw Bayer data or YUV data through on 8-bit output data bus. The center 307,200 (640x480) pixels are active pixels and can be output. The other pixels are used for black level cancelation and interpolation. If no flip in column, column is read out 0 to 647. If flip in column, column is read out from 647 to 0. If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0. In this way, the output pixel color order is always the same.

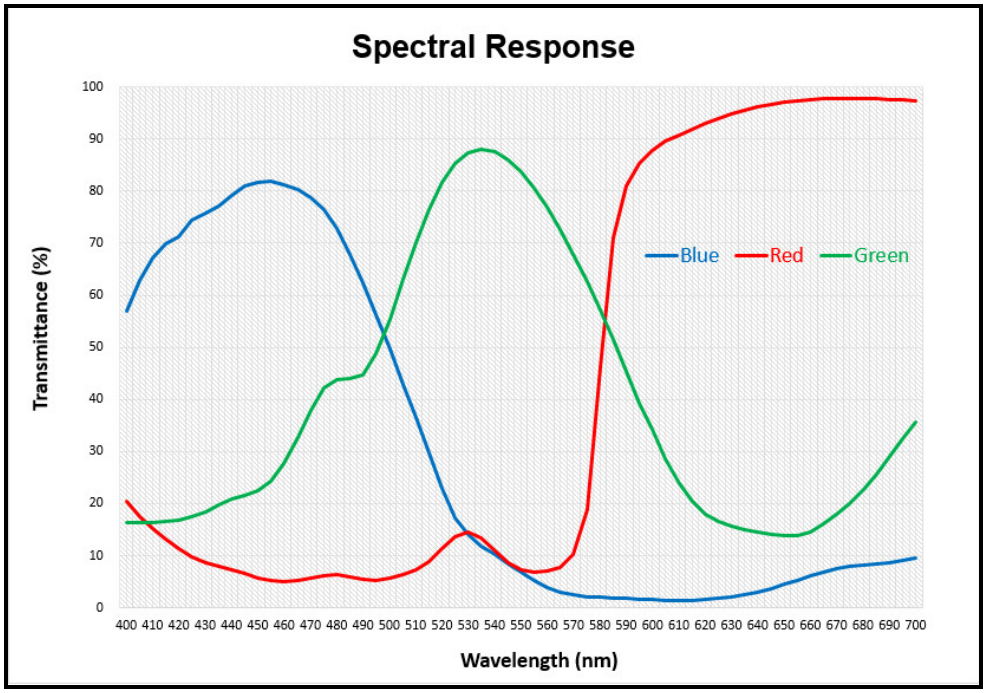


[Figure-02] Sensor array region

2. Color Filter Spectral Characteristics

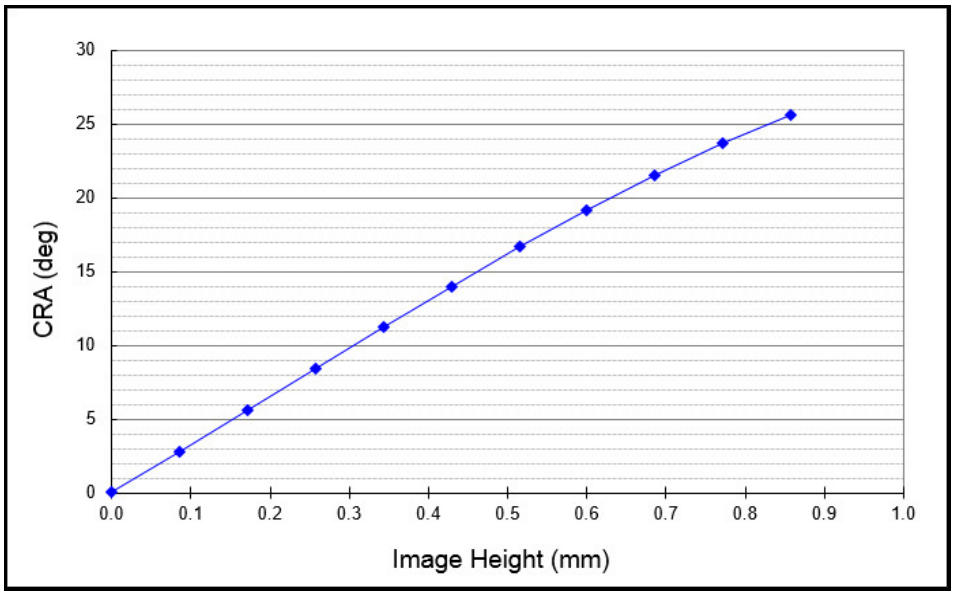
2.1 Spectral Characteristics

[Figure-03] Optical spectrum of color filter



2.2 Chief Ray Angle (CRA)

[Figure-4] Chief Ray Angle Curve



[Table-02] CRA versus Image height plot.

Field (%)	Image Height (mm)	CRA (degree)
0	0	0.02
0.1	0.09	2.79
0.2	0.17	5.6
0.3	0.26	8.42
0.4	0.34	11.23
0.5	0.43	13.98
0.6	0.52	16.69
0.7	0.6	19.19
0.8	0.69	21.53
0.9	0.77	23.71

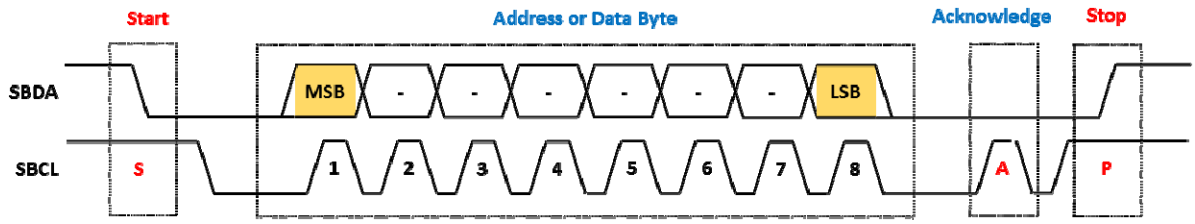
3. Two-wire Serial Bus Communication

The two-wire serial bus interface is controlled by SBCL (serial clock) and SBDA (serial data). The SBCL is driven by the two-wire serial interface master and the SBDA is bi-directional bus. The SBCL and SBDA lines are pulled up to VDDIO by the off-chip register.

3.1 Protocol

3.1.1 Start / Stop condition and the serial address / data byte

[Figure-05] Communication Bus State



Start condition : master device issues the communication start by driving SBDA from "high" to "low" while SBCL is "high".

Stop condition : master device issues the communication stop by driving SBDA from "low" to "high" while SBCL is "high".

Acknowledge/Negative acknowledge : after transmitting each byte, master or slave device issue "acknowledge/negative acknowledge"

3.1.2 Single Write Mode Operation

S	0x86	A	Register Address	A	Data	A	P

3.1.3 Multiple Write Mode Operation (Register address is increased automatically)

S	0x86	A	Register Address	A	Data	A	...	Data	A	P

3.1.4 Single Read Mode Operation

S	0x86	A	Register Address	A	S	0x87	A	Data	/A	P

3.1.5 Multiple Read Mode Operation (Register address is increased automatically)

S	0x86	A	Register Address	A	S	0x87	A	Data	A	...	Data	/A	P

Note 1)

Continuous reading (or writing) increases the register address automatically, if there is no any interrupt.

Note 2)

	From Master to Slave		From Slave to Master		Continuous data reading/writing

0x86 : slave device address 8bit @ write

0x87 : slave device address 8bit @ read

S : Start Condition bit

P : Stop Condition bit

A : Acknowledge bit ('0')

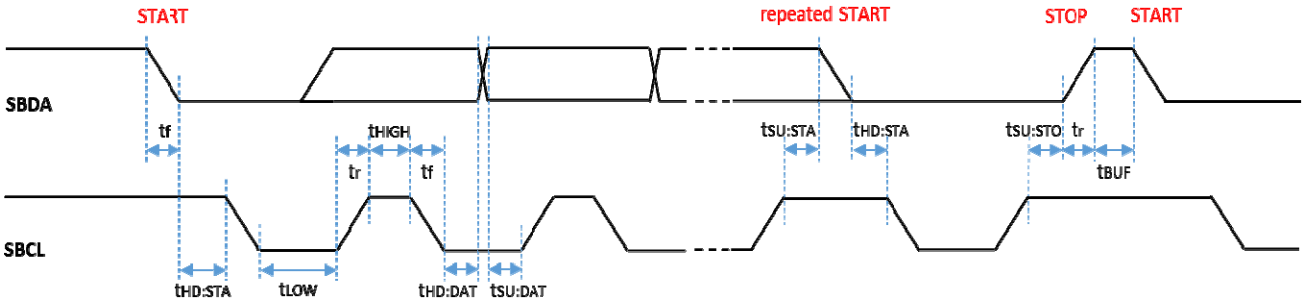
NA : No Acknowledge bit ('1')

Register Address : sensor register address 8bit

Data : sensor register data 8bit @ Nth

3.2 Serial Bus Timing

[Figure-06]



[Table-03]

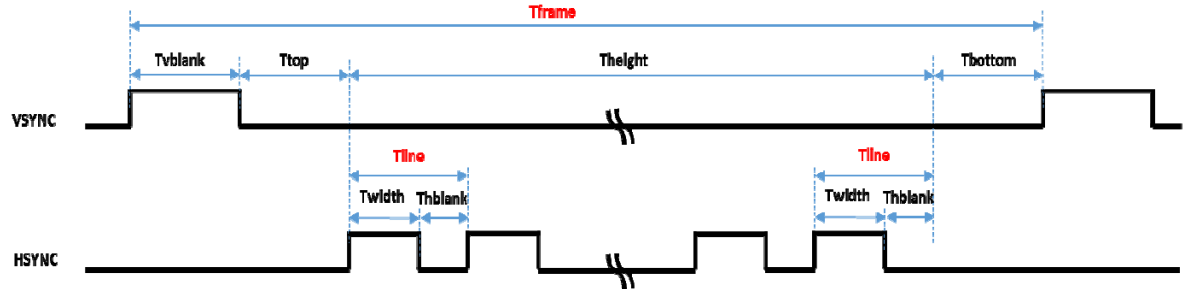
Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	f_{SBCL}		400	KHz
LOW period of the SBCL clock	t_{LOW}	1.3		us
HIGH period of the SBCL clock	t_{HIGH}	0.6		us
Hold time (repeated) START condition	$t_{HD:STA}$	0.6		us
Set-up time for a repeated START condition	$t_{SU:STA}$	0.6		us
Data hold time	$t_{HD:DAT}$	0.3		us
Data set-up time	$t_{SU:DAT}$	0.25		us
Rise time of both SBCL and SBDA signals	t_r		0.3	us
Fall time of both SBCL and SBDA signals	t_f		0.3	us
Set-up time for STOP condition	$t_{SU:STO}$	0.6		us
Bus free time between a STOP and START condition	t_{BUF}	1.3		us

4. Application

4.1 Timing

Frame Timing is controlled by HBNKT (horizontal blank, page #0 : 0x31 & 0x32) and VBNKT (vertical blank, page #0 : 0x33 & 0x34) registers. The timing is shown below. The VSYNC is supposed to be active low and HSYNC is active high.

[Figure-07]



Tframe = Tvblank + Ttop + Theight + Tbottom

Tframe : one frame time (unit : line)

Tvblank : vertical blank time, 5 + VBNKT (set by register page #0 : 0x33 & 0x34)

Ttop : vertical top dummy time, 8 @ VGA

Theight : valid line time, 480 @ VGA

Tbottom : vertical bottom dummy time, 0 @ VGA

If the exposure time is less than the Tframe, then the frame rate is controlled by (Tvblank + Theight). If the exposure time is over the Tframe, then the frame rate is controlled by EXPTIME (page #24 : 0x30 & 0x31)

Tline = Twidth + Thblank

Tline : one line time (unit : the period of TCR_CLK that is internal clock to process one pixel)

Twidth : valid pixel time (1 line), 640 @ VGA

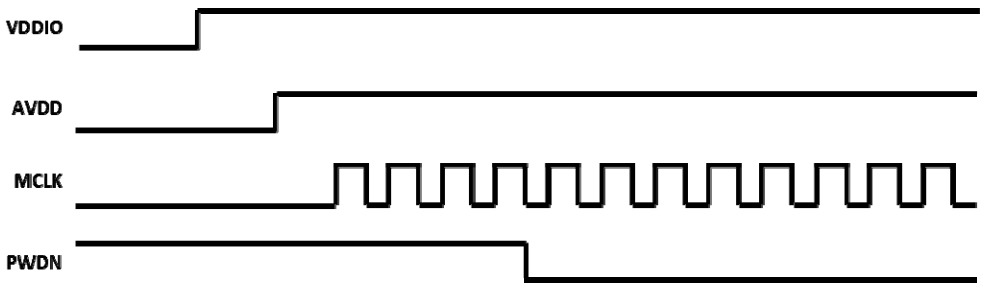
Thblank : horizontal blank time, Tdelay + HBNKT (set by register page #0 : 0x31 & 0x32)

Tdelay : horizontal delay, 152 @ VGA

4.2 Power on/off Sequence

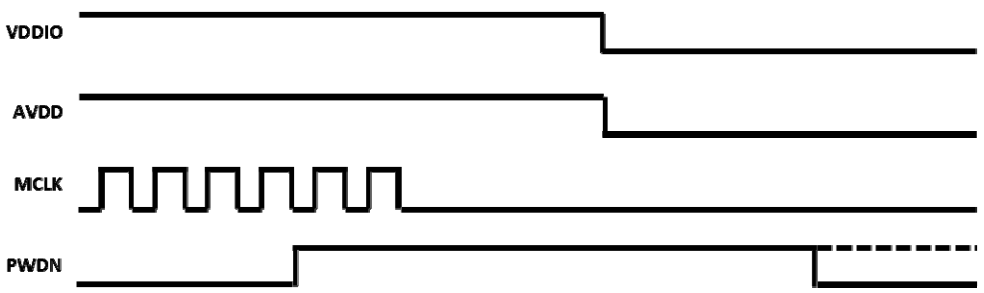
4.2.1 Power on

[Figure-08]



4.2.2 Power off

[Figure-09]



5. Electrical Definitions and Characteristics

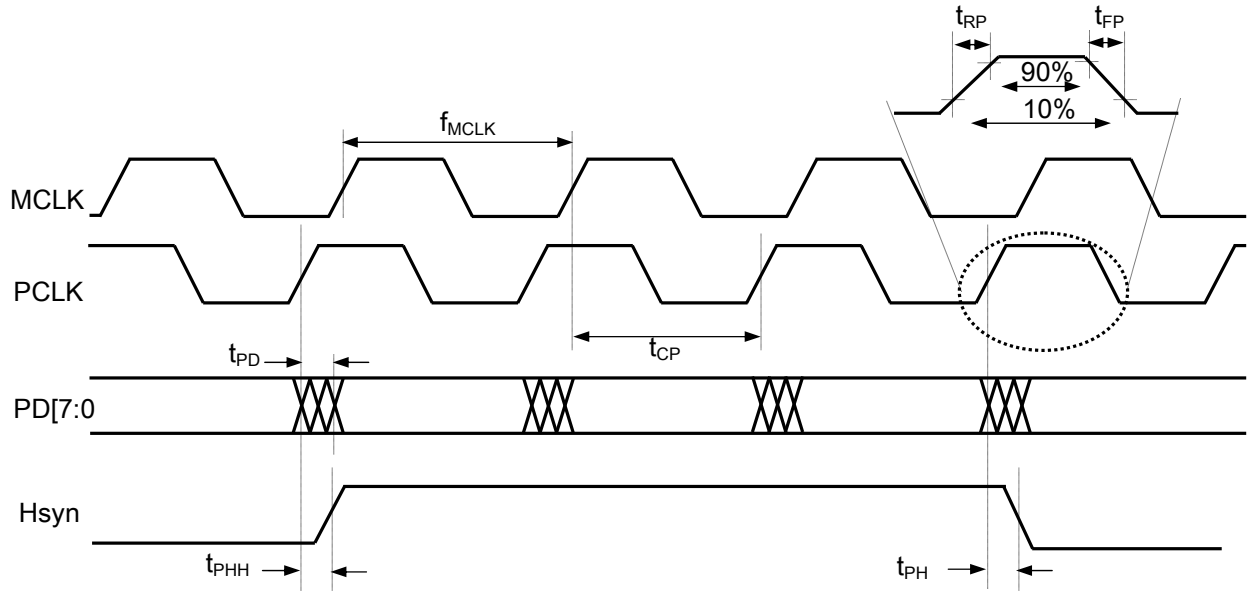
5-1. DC Electrical Parameters

[Table-04] : DC Electrical Definitions and Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
AVDD	Analog Power Supply		2.7	2.8	3	V
VDDIO	Digital I/O Power Supply		1.7	2.8(1.8)	3	V
VDD	Core Power Supply		1.7	1.8	1.9	V
IAVDD	Analog Operating Current			TBD		
IVDDIO	Digital I/O Operating Curenet	1.8V		TBD		mA
		2.8V		TBD		mA
IVDD	Digial Core Opearing Current			TBD		mA
ISTBY1	Analog StandBy Current			TBD		uA
ISTBY2	Digital I/O and Core StandBy Current			TBD		uA
VIH	Input High Voltage	VDDIO=2.8V	0.7*VDDIO			V
		VDDIO=1.8V	0.7*VDDIO			V
VIL	Input Low Voltage	VDDIO=2.8V			0.3*VDDIO	V
		VDDIO=1.8V			0.3*VDDIO	V
VOH	Output High Voltage	VDDIO=2.8V	0.8*VDDIO			V
		VDDIO=1.8V	0.8*VDDIO			V
VOL	Out Low Voltage	VDDIO=2.8V			0.2*VDDIO	V
		VDDIO=1.8V			0.2*VDDIO	V

5-2 AC Electrical Parameters

[Figure-10] I/O Timing Diagram



[Table-05] AC Electrical Definitions and Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
Fmclk	Input Clock Frequency			24		MHz
tRP	Pixel Clock Rise Time	Default		TBD		
tFP	Pixel Clock Fall Time	Default		TBD		
tPD	Pixel Clock to Data Delay	Default	0.38	0.52	0.75	ns
tPHH	Pixel clock to Hsync High	Default	0.48	0.61	0.81	ns
tPHL	Pixel clock to Hsync Low	Default	0.63	0.78	1.02	ns
tCP	Input Clock to Pixel Clock delay	Default	23.6	25.5	28.9	ns
Cload	Output Load Capcaitance	Default		20		pF

6. Register List

Page 0x00 (Global Block) : Global Operation Control

Address	Register Name	Default Value	R/W	Description
0x00	**PAGE_ SEL**	**0x00**	**RW**	[4:0] Page Address Selection 0x00 ('d0) Global control 0x01 ('d1) Analog Timing Control 0x08 (d8) Pre-Processing 0x0A ('d10) Lens Shading 0x0C ('d12) Bayer Domain 0x0E ('d14) Color 0x10 ('d16) Gamma 0x12 ('d18) Image Enhancement 0x18 ('d24) AEC/AGC 0x1A ('d26) AWB ETC. Reserved
0x01	**CHIP_ID0**	**0x63**	**RO**	Chip ID 0
0x02	**CHIP_ID1**	**0x02**	**RO**	Chip ID 1
0x03	**CHIP_ID2**	**0x00**	**RO**	Chip ID 2
0x04	**CHIP_ID3**	**0x00**	**RO**	Chip ID 3
0x08	**CHIP_CTRL1**	**0x00**	**RW**	[0] Global Software Reset Enable
0x09	**CHIP_CTRL2**	**0x01**	**RW**	[1] Sync./Data PAD Output Enable [0] Sensor Power Down Mode enable
0x10	**PAD_CTRL1**	**0x22**	**RW**	[6:4] PCLK PAD Drive Current Select 0 0 0 0 mA 0 0 1 2 mA 0 1 0 4 mA

<table>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>0</td><td>1</td><td>1</td><td>6 mA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8 mA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10 mA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 mA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>14 mA</td></tr>
</table>
[2:0] Sync./Data PAD Drive Current Select
<table>
<tr><td>0</td><td>0</td><td>0</td><td>0 mA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2 mA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4 mA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>6 mA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8 mA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10 mA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 mA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>14 mA</td></tr>
</table>
</td></tr>
<tr><td>0x11</td><td>PAD_CTRL2</td><td>0x02</td><td>RW</td><td>
[2:0] SBDA PAD Drive Current Select
<table>
<tr><td>0</td><td>0</td><td>0</td><td>0 mA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2 mA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4 mA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>6 mA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8 mA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10 mA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 mA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>14 mA</td></tr>
</table>
</td></tr>
<tr><td>0x20</td><td>OPER_CTRL1</td><td>0x00</td><td>RW</td><td>[0] Sensor Operation enable</td></tr>
<tr><td>0x21</td><td>OPER_CTRL2</td><td>0x00</td><td>RW</td><td>
[3:2] Internal frequency division
<table>
<tr><td>0</td><td>0</td><td>1/1 MCLK</td></tr>
<tr><td>0</td><td>1</td><td>1/2 MCLK</td></tr>
<tr><td>1</td><td>0</td><td>1/4 MCLK</td></tr>
<tr><td>1</td><td>1</td><td>1/8 MCLK</td></tr>
</table>
[1] Vertical mirror enable
[0] Horizontal mirror enable
</td></tr>
<tr><td>0x30</td><td>MODE_FORM</td><td>0x00</td><td>RW</td><td>
[0] Pixel Video Format mode
<table>
<tr><td>0</td><td>VGA (640 x 480)</td></tr>
<tr><td>1</td><td>QVGA (320 x 240)</td></tr>
</table>
</td></tr>
<tr><td>0x31</td><td>HBNKT_H</td><td>0x00</td><td>RW</td><td>[3:0] horizontal blank upper byte</td></tr>
<tr><td>0x32</td><td>HBNKT_L</td><td>0x07</td><td>RW</td><td>[7:0] horizontal blank lower byte (Unit : Pixel Clock)</td></tr>
<tr><td>0x33</td><td>VBNKT_H</td><td>0x00</td><td>RW</td><td>[3:0] vertical blank upper byte</td></tr>
</table>

0x34	**VBNKT_L**	**0x07**	**RW**	[7:0] vertical blank lower byte (Unit : Row line)
0x60	**OPOLARITY**	**0x16**	**RW**	[4] : PCLK_SEL, PCLK out @ V/H-blank 0 : PCLK output enable during data output valid 1 : PCLK output enable during data output valid & V-blank & H-blank [2] : VSYNC_POL, V-Sync polarity control 0 : V-sync 'L' output during V-blank, 'H' during else 1 : V-sync 'H' output during V-blank, 'L' during else [1] : HSYNC_POL, H-Sync polarity control 0 : H-sync 'L' output during data output valid, 'H' during else 1 : H-sync 'H' output during data output valid, 'L' during else [0] : PCLK_POL, PCLK polarity control 0 : PCLK falling edge @ H-sync enable edge & 1'st data output 1 : PCLK rising edge @ H-sync enable edge & 1'st data output
0x68	**OFORMAT**	**0x03**	**RW**	[1] Y first selection enable [0] U first selection enable
0x70	**WINCTRL**	**0x89**	**RW**	[7:6] windowing width upper byte [4] windowing height upper byte [0] windowing enable
0x71	**WINROWS**	**0x00**	**RW**	[7:0] windowing row start
0x72	**WINHEIGHT**	**0xFF**	**RW**	[7:0] windowing height lower byte
0x73	**WINCOLS**	**0x00**	**RW**	[7:0] windowing column start
0x74	**WINWIDTH**	**0xFF**	**RW**	[7:0] windowing width lower byte

Page 0x01 (Analog Block) : Analog Timing Control				
Address	**Register Name**	**Default Value**	**R/W**	**Description**
0x40	**LDO_CTRL1**	**0x01**	**RW**	[7] Internal Core LDO enable 0 : LDO enable, 1 : LDO disable

Page 0x08 (Pre-processing block)				
Address	**Register Name**	**Default Value**	**R/W**	**Description**
0x10	**GAINCTRL**	**0x03**	**RW**	[1] White balancing gain enable [0] Global digital gain enable
0x80	**BLCCTRL**	**0x01**	**RW**	[0] Black level calibration enable
0x81	**FIXBLC**	**0x00**	**RW**	[7:0] Fixed black level value For +/- arithmetic, use 2's complement value
0x88	**DRKVH**	**0x00**	**RO**	MSB of dark level value [7:6] Red channel in even line [5:4] Green channel in even line [3:2] Green channel in odd line [1:0] Blue channel in odd line
0x89	**DRKVLR**	**0x00**	**RO**	[7:0] LSB of dark level value of red channel in even line
0x8A	**DRKVLGR**	**0x00**	**RO**	[7:0] LSB of dark level value of green channel in even line
0x8B	**DRKVLGB**	**0x00**	**RO**	[7:0] LSB of dark level value of green channel in odd line
0x8C	**DRKVLB**	**0x00**	**RO**	[7:0] LSB of dark level value of blue channel in odd line
0xE0	**ISPOPTION**	**0x80**	**RW**	[0] BLC update selection 0: always, 1: BLC update stop @ AEG stop flag
0xE8	**TESTFUN**	**0x00**	**RW**	Digital pattern generation register [6] Horizontal ramping generation [5] Fixed value generation [3] Color bar generation [0] Ramping signal generation option 0: 10bit, 1: 8bit
0xE9	**TESTDATH**	**0x02**	**RW**	[1:0] MSB of digital pattern value
0xEA	**TESTDATL**	**0x86**	**RW**	[7:0] LSB of digital pattern value
0xEF	**PREGAIN**	**0x80**	**RW**	[7:0] Global pre-gain value (x1/128)

Page 0x0A (LSC block)

Address	Register Name	Default Value	R/W	Description
0x10	LSCCTRL	0x01	RW	[0] Lens shading correction enable
0x28	LRCORNERR	0x00	RW	[7:4] LSC left corner R Gain [3:0] LSC right corner R Gain
0x29	TBCORNERR	0x00	RW	[7:4] LSC top corner R Gain [3:0] LSC bottom corner R Gain
0x2A	LRCORNERG	0x00	RW	[7:4] LSC left corner G Gain [3:0] LSC right corner G Gain
0x2B	TBCORNERG	0x00	RW	[7:4] LSC top corner G Gain [3:0] LSC bottom corner G Gain
0x2C	LRCORNERB	0x00	RW	[7:4] LSC left corner B Gain [3:0] LSC right corner B Gain
0x2D	TBCORNERB	0x00	RW	[7:4] LSC top corner B Gain [3:0] LSC bottom corner B Gain
0x30	LSCGGA	0x00	RW	[7:4] LSC global Gain 1 [3:0] LSC global Gain 2
0x31	LSCGGB	0x00	RW	[7:4] LSC global Gain 3 [2:0] LSC global Gain 4 (Max value 5, 101b)
0xE0	LSCBASE	0x04	RW	[3:2] MSB of LSC Center X coordinate [1:0] MSB of LSC Center Y coordinate
0xE1	LSCBASEX	0x44	RW	[7:0] LSB of LSC Center X coordinate
0xE2	LSCBASEY	0xF4	RW	[7:0] LSB of LSC Center Y coordinate

Page 0x0C (DPC & LPF block)				
Address	**Register Name**	**Default Value**	**R/W**	**Description**
0x10	DPCCTRL	0x01	R/W	[0] Dead pixel concealment enable
0x11	DPCOPTION	0x11	R/W	[6] Green channel mixing option [3:0] DPC mode divider value
0x18	DPCTH	0x04	R/W	[7:0] Defective pixel detection range value
0x19	DPCTHSLOPE	0x01	R/W	[4:0] Defective pixel detection range decreasing slope
0x80	LPFCTRL	0x01	R/W	[0] LPF enable
0x81	LPFOPTION	0x43	R/W	[7] Manual increasing threshold option [5] Green channel mixing option

				[4] Adaptive threshold value option for low level [3:0] Additional threshold option for R/B channel
0x88	**LPFTH0**	**0x04**	**R/W**	[7:0] Initial threshold value
0x89	**LPFTHSLOPE1**	**0x04**	**R/W**	[7:0] LPF threshold increase slope 1
0x8A	**LPFTHSLOPE2**	**0x20**	**R/W**	[7:0] LPF threshold increase slope 2
0x8B	**LPFTH1**	**0x05**	**R/W**	[7:0] Additional global threshold 1 value
0x8C	**LPFTH2**	**0x08**	**R/W**	[7:0] Additional global threshold 2 value
0xE0	**OUT2NOR**	**0x10**	**R/W**	[7:0] Outdoor to normal condition point
0xE1	**NOR2DARK**	**0x40**	**R/W**	[7:0] Normal to dark condition point

Page 0x0E (Color domain block)

Address	Register Name	Default Value	R/W	Description
0x10	**INTCTRL**	**0x01**	**R/W**	[0] Color interpolation enable
0x11	**INTOPTION**	**0x48**	**R/W**	[6] Edge sensing mode W [5] G-LPF option [4:0] Flat detection threshold value
0x12	**INTDETAL**	**0x0B**	**R/W**	[7:5] Additional threshold option for flat detection [4:0] Detail detection threshold
0x80	**CMCCTRL**	**0x01**	**R/W**	[0] Color correction enable
0x90	**CMCOPTION**	**0x33**	**R/W**	[7] Automatic CMC condition enable [5] Sign Bit of CMC12 [4] Sign Bit of CMC13 [3] Sign Bit of CMC21 [2] Sign Bit of CMC23 [1] Sign Bit of CMC31 [0] Sign Bit of CMC32
0x91	**CMC11**	**0x3B**	**R/W**	[6:0] Color correction coefficient 11
0x92	**CMC12**	**0xCE**	**R/W**	[6:0] Color correction coefficient 12
0x93	**CMC13**	**0xF7**	**R/W**	[6:0] Color correction coefficient 13
0x94	**CMC21**	**0x13**	**R/W**	[6:0] Color correction coefficient 21
0x95	**CMC22**	**0x25**	**R/W**	[6:0] Color correction coefficient 22
0x96	**CMC23**	**0x08**	**R/W**	[6:0] Color correction coefficient 23

0x97	CMC31	0xF2	R/W	[6:0] Color correction coefficient 31
0x98	CMC32	0xC7	R/W	[6:0] Color correction coefficient 32
0x99	CMC33	0x47	R/W	[6:0] Color correction coefficient 33
0xA1	CMCOFS11	0x01	R/W	[7:0] Color offset coefficient 11 (use 2's complement for minus offset)
0xA2	CMCOFS12	0x00	R/W	[7:0] Color offset coefficient 12 (use 2's complement for minus offset)
0xA3	CMCOFS13	0xFF	R/W	[7:0] Color offset coefficient 13 (use 2's complement for minus offset)
0xA4	CMCOFS21	0xFF	R/W	[7:0] Color offset coefficient 21 (use 2's complement for minus offset)
0xA5	CMCOFS22	0x00	R/W	[7:0] Color offset coefficient 22 (use 2's complement for minus offset)
0xA6	CMCOFS23	0x01	R/W	[7:0] Color offset coefficient 23 (use 2's complement for minus offset)
0xA7	CMCOFS31	0xFB	R/W	[7:0] Color offset coefficient 31 (use 2's complement for minus offset)
0xA8	CMCOFS32	0xEF	R/W	[7:0] Color offset coefficient 32 (use 2's complement for minus offset)
0xA9	CMCOFS33	0x16	R/W	[7:0] Color offset coefficient 33 (use 2's complement for minus offset)

Page 0x10 (Gamma block)

Address	Register Name	Default Value	R/W	Description
0x10	GAMMACTRL	0x01	R/W	[0] Gamma correction enable
0x20	GAMMA00	0x00	R/W	[7:0] Gamma correction output point 0 (0 code of 10bit)
0x21	GAMMA01	0x04	R/W	[7:0] Gamma correction output point 1 (16 code of 10bit)
0x22	GAMMA02	0x0B	R/W	[7:0] Gamma correction output point 2 (32 code of 10bit)
0x23	GAMMA03	0x24	R/W	[7:0] Gamma correction output point 3 (64 code of 10bit)
0x24	GAMMA04	0x49	R/W	[7:0] Gamma correction output point 4 (128 code of 10bit)
0x25	GAMMA05	0x66	R/W	[7:0] Gamma correction output point 5 (192

				code of 10bit)
0x26	**GAMMA06**	**0x7C**	**R/W**	[7:0] Gamma correction output point 6 (256 code of 10bit)
0x27	**GAMMA07**	**0x8D**	**R/W**	[7:0] Gamma correction output point 7 (320 code of 10bit)
0x28	**GAMMA08**	**0x9B**	**R/W**	[7:0] Gamma correction output point 8 (384 code of 10bit)
0x29	**GAMMA09**	**0xAA**	**R/W**	[7:0] Gamma correction output point 9 (448 code of 10bit)
0x2A	**GAMMA10**	**0xB6**	**R/W**	[7:0] Gamma correction output point 10 (512 code of 10bit)
0x2B	**GAMMA11**	**0xCA**	**R/W**	[7:0] Gamma correction output point 11 (640 code of 10bit)
0x2C	**GAMMA12**	**0xDC**	**R/W**	[7:0] Gamma correction output point 12 (768 code of 10bit)
0x2D	**GAMMA13**	**0xEF**	**R/W**	[7:0] Gamma correction output point 13 (896 code of 10bit)
0x2E	**GAMMA14**	**0xF8**	**R/W**	[7:0] Gamma correction output point 14 (1023 code of 10bit)

Page 0x12 (Image Enhancement block)

Address	Register Name	Default Value	R/W	Description
0x10	**EDGCTRL**	**0x01**	**R/W**	[0] Edge enhancement enable
0x20	**POSGAIN**	**0x20**	**R/W**	[5:0] Edge enhancement positive gain (x1/16)
0x21	**NEGGAIN**	**0x20**	**R/W**	[5:0] Edge enhancement negative gain (x1/16)
0x22	**VCORE**	**0x22**	**R/W**	[7:4] Edge enhancement positive core value [3:0] Edge enhancement negative core value
0x23	**POSCLIP**	**0xFF**	**R/W**	[6:0] Edge enhancement positive maximum value
0x24	**NEGCLIP**	**0xFF**	**R/W**	[6:0] Edge enhancement negative maximum value
0x29	**ADAPEMAX**	**0x10**	**R/W**	[7:0] Adaptive edge gain reference start point
0x2A	**ADAPEVGAIN**	**0x88**	**R/W**	[7] Adaptive edge gain enable [3:0] Adaptive edge gain increasing slope (x1/8)

0x2E	**AUTOEPNT**	**0x38**	**R/W**	[7:0] Automatic edge suppression start point
0x2F	**AUTOESLOPE**	**0x10**	**R/W**	[7:4] Automatic edge suppression decreasing slope [3:0] Automatic edge suppression end gain value
0x50	**EVCCTRL**	**0x02**	**R/W**	[7] Edge mode H enable [6] Edge mode H u-value divider 0: x1/4, 1: x1/2 [5] Edge mode H s-max divider 0: x1/4, 1: x1/2 [3:0] Edge mode H e-value threshold point
0x51	**EVCYLVLL**	**0x80**	**R/W**	[7:0] Edge mode H u-value increasing start point
0x52	**EVCYLVLH**	**0xC9**	**R/W**	[7:0] Edge mode H u-value decreasing start point
0x53	**EVCYMAX**	**0x80**	**R/W**	[7:0] Edge mode H s-max increasing start point
0x54	**EVCOPTION**	**0x08**	**R/W**	[7] High-light increasing edge without reducing for H point [5] High-light edge mode enable in negative edge [4] High-light edge mode enable in positive edge [2:0] Edge mode H maximum rate (x1)
0x60	**CSUPCTRL**	**0x00**	**R/W**	[7] Maximum value to suppress a false color on edge [5:3] Blue color subtraction value [2:0] Red color subtraction value
0x61	**CSUPONEDGE**	**0x82**	**R/W**	[7:4] Slope to suppress a false color on edge 3:0 Initial point to suppress a false color on edge
0x80	**IEFFECT**	**0x00**	**R/W**	[4] Embossing mode [3] Sketch mode [2] Inverse image mode [1] Fixed CB/CR value mode [0] Color improvement enable

0x88	CBFIXVAL	0x60	R/W	[7:0] Blue color fixed value
0x89	CRFIXVAL	0xA0	R/W	[7:0] Red color fixed value
0x8E	AUTOSPNT	0x38	R/W	[7:0] Automatic color suppression start point
0x8F	AUTOSSLOPE	0x10	R/W	[7:4] Automatic color suppression decreasing slope [3:0] Automatic color suppression end gain value
0x90	CONTRAST	0x10	R/W	[7:0] Luminance contrast control gain
0x91	BRIGHTNESS	0x00	R/W	[7:0] Brightness control value (2's complement)
0x92	BRGTMAX	0xFF	R/W	[7:0] Luminance output maximum value
0x93	BRGTMIN	0x00	R/W	[7:0] Luminance output minimum value
0x98	CBSUGAIN	0x10	R/W	[7:0] Blue color saturation upper gain
0x99	CRSUGAIN	0x10	R/W	[7:0] Red color saturation upper gain
0x9A	CBSDGAIN	0x10	R/W	[7:0] Blue color saturation lower gain
0x9B	CRSDGAIN	0x10	R/W	[7:0] Red color saturation lower gain
0x9C	CBVALMAX	0xFF	R/W	[7:0] Blue color maximum value
0x9D	CBVALMIN	0x00	R/W	[7:0] Blue color minimum value
0x9E	CRVALMAX	0xFF	R/W	[7:0] Red color maximum value
0x9F	CRVALMIN	0x00	R/W	[7:0] Red color minimum value

Page 0x18 (AEGC block)

Address	Register Name	Default Value	R/W	Description
0x10	AEGCTRL	0x80	RW	[7] Automatic exposure & gain control enable
0x18	LOCKRANGE	0x00	RW	[1:0] Lock range selection
0x20	EXPTSTEP	0x7D	RW	[7:0] Exposure step control value for anti-flicker
0x21	EXPTSTEPMAX	0x0F	RW	[5:0] Frame control for automatic exposure control
0x30	EXPTIMEH	0x00	RW	[4:0] MSB of internal exposure time
0x31	EXPTIMEL	0x7D	RW	[7:0] LSB of internal exposure time
0x32	GCGAIN	0x00	RW	[1:0] Global analog gain value
0x33	GFGAIN	0x28	RW	[7:0] Global digital gain value
0x51	GAINMAX	0x48	RW	[7:0] Maximum gain value in AGC

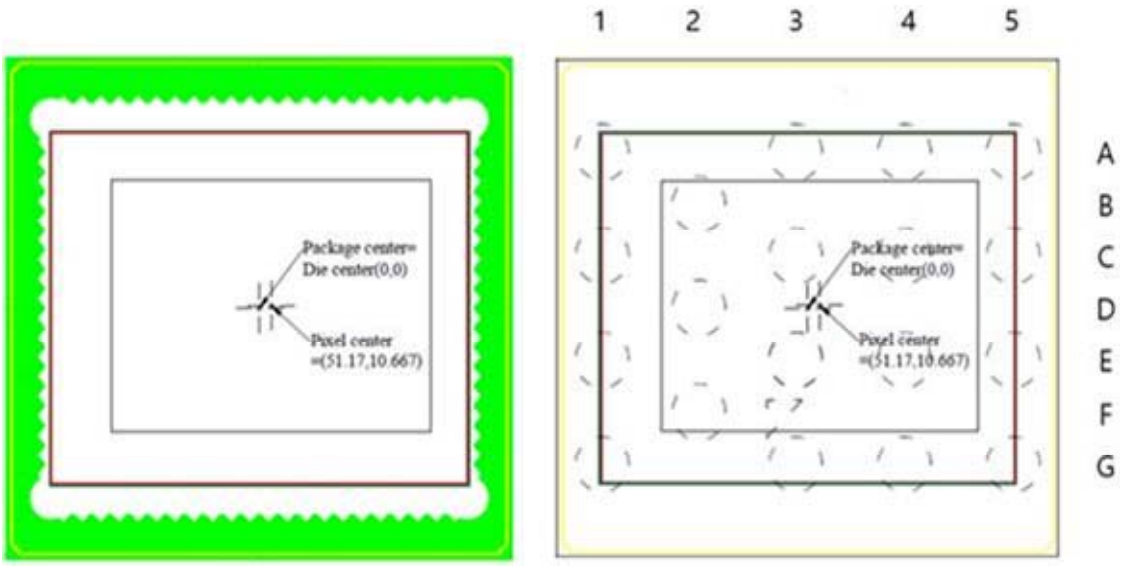
0x52	GAINMIN	0x08	RW	[7:0] Minimum gain value in AGC
0x80	YLEVEL4N	0x78	RW	[7:0] Luminance level to converge in normal condition
0x82	YLEVEL4D	0x70	RW	[7:0] Luminance level to converge in dark condition
0xA0	WCTRL	0x00	RW	[1:0] Weight mode to calculate an average luminance value

Page 0x1A (AWB block)				
Address	**Register Name**	**Default Value**	**R/W**	**Description**
0x10	AWBCTRL	0xb3	RW	[7] Automatic White balancing enable
0x20	CBLEVEL	0x80	RW	[7:0] Cb level to converge
0x21	CRLEVEL	0x80	RW	[7:0] Cr level to converge
0x30	RGMAX	0x6F	RW	[7:0] Maximum of RGAIN
0x31	RGMIN	0x38	RW	[7:0] Minimum of RGAIN
0x32	BGMAX	0x6F	RW	[7:0] Maximum of BGAIN
0x33	BGMIN	0x3C	RW	[7:0] Minimum of BGAIN
0x40	ENTERBRT	0x04	RW	[7:0] Threshold of exposure time to enter bright condition
0x41	OUTBRT	0x08	RW	[7:0] Threshold of exposure time to get out bright condition
0x42	RGBRT	0x5C	RW	[7:0] RGAIN at bright condition
0x43	BGBRT	0x5A	RW	[7:0] BGAIN at bright condition
0x50	RGINTO_N	0x48	RW	[7:0] R gain boundary value to change light source of high color temperature
0x51	BGINTO_N	0x58	RW	[7:0] B gain boundary value to change light source of high color temperature
0x52	RGINTO_L	0x48	RW	[7:0] R gain boundary value to change light source of low color temperature
0x53	BGINTO_L	0x58	RW	[7:0] B gain boundary value to change light source of low color temperature
0x60	RGAIN	0xb0	RW	[7:0] RGAIN
0x61	BGAIN	0xb5	RW	[7:0] BGAIN
0x62	GGAIN	0x80	RW	[7:0] GGAIN
0x80	CBMAX4W	0x48	RW	[7:0] Maximum Cb of white pixel

0x81	**CBMIN4W**	**0x38**	**RW**	[7:0] Minimum Cb of white pixel
0x82	**CRMAX4W**	**0x48**	**RW**	[7:0] Maximum Cr of white pixel
0x83	**CRMIN4W**	**0x38**	**RW**	[7:0] Minimum Cr of white pixel
0x84	**CXMAX4W**	**0x48**	**RW**	[7:0] Maximum Cb, Cr average of white pixel
0x85	**CXMIN4W**	**0x38**	**RW**	[7:0] Minimum Cb, Cr average of white pixel
0x86	**YMAX4W**	**0x6C**	**RW**	[7:0] Maximum Y of white pixel
0x87	**YMIN4W**	**0x38**	**RW**	[7:0] Minimum Y of white pixel
0x88	**WCNTTH**	**0x05**	**RW**	[7:0] Threshold number of white pixels
0x89	**WCNTMIN**	**0x30**	**RW**	[7:0] Minimum count of white pixels in a frame

7. IT03A1 Pin Description

7.1 CSP package top view (unit: um)



[Figure-11]

7.2 CSP ball description

[Table-06]

	1	2	3	4	5
A	VDD	/	PD[0]	PD[2]	PCLK
B	/	PD[4]	/	/	/
C	VDDIO	/	HSYNC	PD[3]	PD[1]
D	/	VSS	/	/	/
E	SBCL	/	VSYNC	PD[7]	PD[5]
F	/	SBDA	/	/	/
G	AVDD	/	PWDN	PD[6]	MCLK

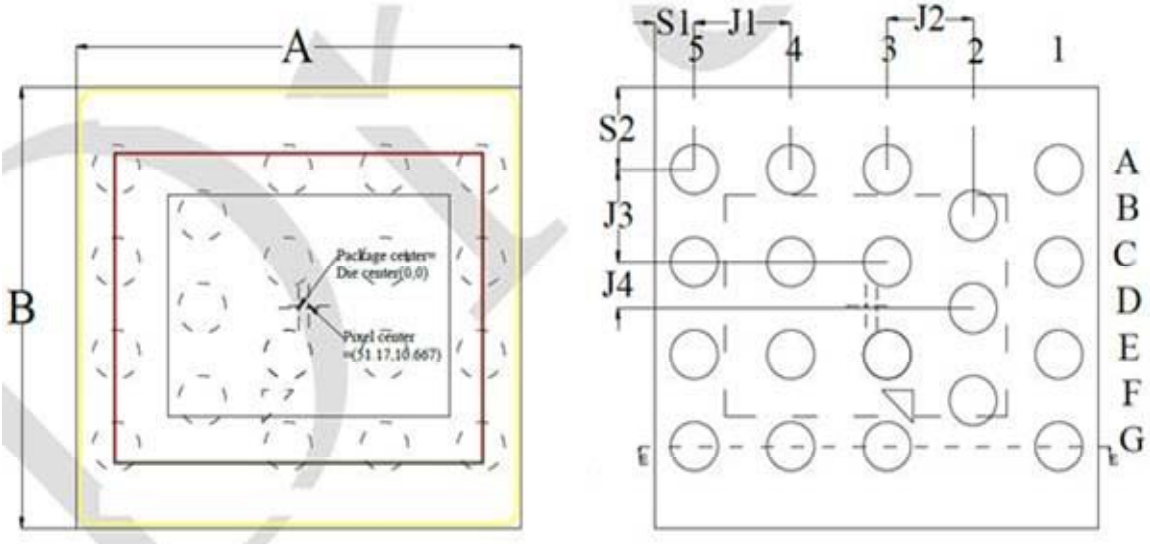
7.3 CSP pin description

[Table-07]

Ball	Name	Function	Ball Coordinate	
			X	Y
A1	VDD	Digital Core Power (1.8V)	0.1935	1.6700
C1	VDDIO	Digital I/O Power (1.8V ~ 2.8V)	0.1935	1.2400
E1	SBCL	Serial Bus Clock	0.1935	0.8100
G1	AVDD	Analog Power (2.8V)	0.1935	0.3800
B2	PD4	Data Out[4]	0.6115	1.4550
D2	VSS	Digital IO / Core Ground	0.6115	1.0250
F2	SBDA	Serial Bus Data	0.6115	0.5950
A3	PD0	Data Out[0]	1.0295	1.6700
C3	HSYNC	Horizontal Synchronization	1.0295	1.2400
E3	VSYNC	Frame Synchronous Signal	1.0295	0.8100
G3	PWDN	Chip Select Signal. (Active Low)	1.0295	0.3800
A4	PD2	Data Out[2]	1.4995	1.6700
C4	PD3	Data Out[3]	1.4995	1.2400
E4	PD7	Data Out[7]	1.4995	0.8100
G4	PD6	Data Out[6]	1.4995	0.3800
A5	PCLK	Output Pixel Data Synchronous Clock	1.9695	1.6700
C5	PD1	Data Out[1]	1.9695	1.2400
E5	PD5	Data Out[5]	1.9695	0.8100
G5	MCLK	Sensor Chip Master Clock	1.9695	0.3800

7.4 CSP Package mechanical drawing (unit : um)

[Figure-12]



[Table-08]

Parameter	Symbol	Nominal	Min	Nax	Nominal	Min	Nax
		Milimeters			Inches		
Package Body Dimension X	A	2.163	2.138	2.188	0.085	0.084	0.086
Package Body Dimension Y	B	2.050	2.025	2.075	0.081	0.080	0.082
Package Height	C	0.690	0.635	0.745	0.027	0.025	0.029
Ball Diameter	D	0.230	0.200	0.260	0.009	0.008	0.010
Total Ball Count	N	20					
Ball Count X axis	N1	5					
Ball Count Y axis	N2	7					
Pins Pitch X axis-1	J1	0.4700			0.01850		
Pins Pitch X axis-2	J2	0.4180			0.01646		
Pins Pitch Y axis-1	J3	0.4300			0.01693		
Pins Pitch Y axis-2	J4	0.2150			0.00846		
Edge to Ball Center Distance along X	S1	0.1935	0.1635	0.2235	0.00762	0.00644	0.00880
Edge to Ball Center Distance along X	S2	0.3800	0.3500	0.4100	0.01496	0.01378	0.01614

8. Revision History

Rev	Remark	Date
0	Initial Release	1st Sep. 2014