

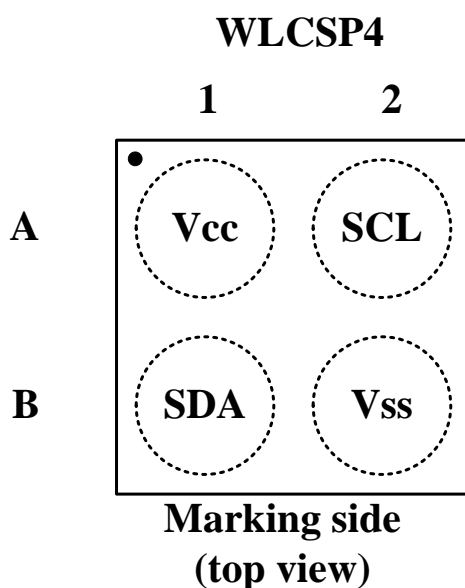
Features

- Compatible with all data transfer protocol
 - 1 MHz
 - 400 kHz
 - 100 kHz
- Memory array:
 - 128 Kbit (16 Kbytes) of EEPROM
 - Page size: 64 bytes
- Single supply voltage and high speed:
 - 1 MHz
- Write:
 - Byte Write within 3 ms
 - Page Write within 3 ms
- Operating Ambient Temperature:
 - From -40 °C up to +85 °C
- High-reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
- Internally Organized:
 - BL24C128A, 16,384 X 8 (128K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- WLCSP4 packages

Description

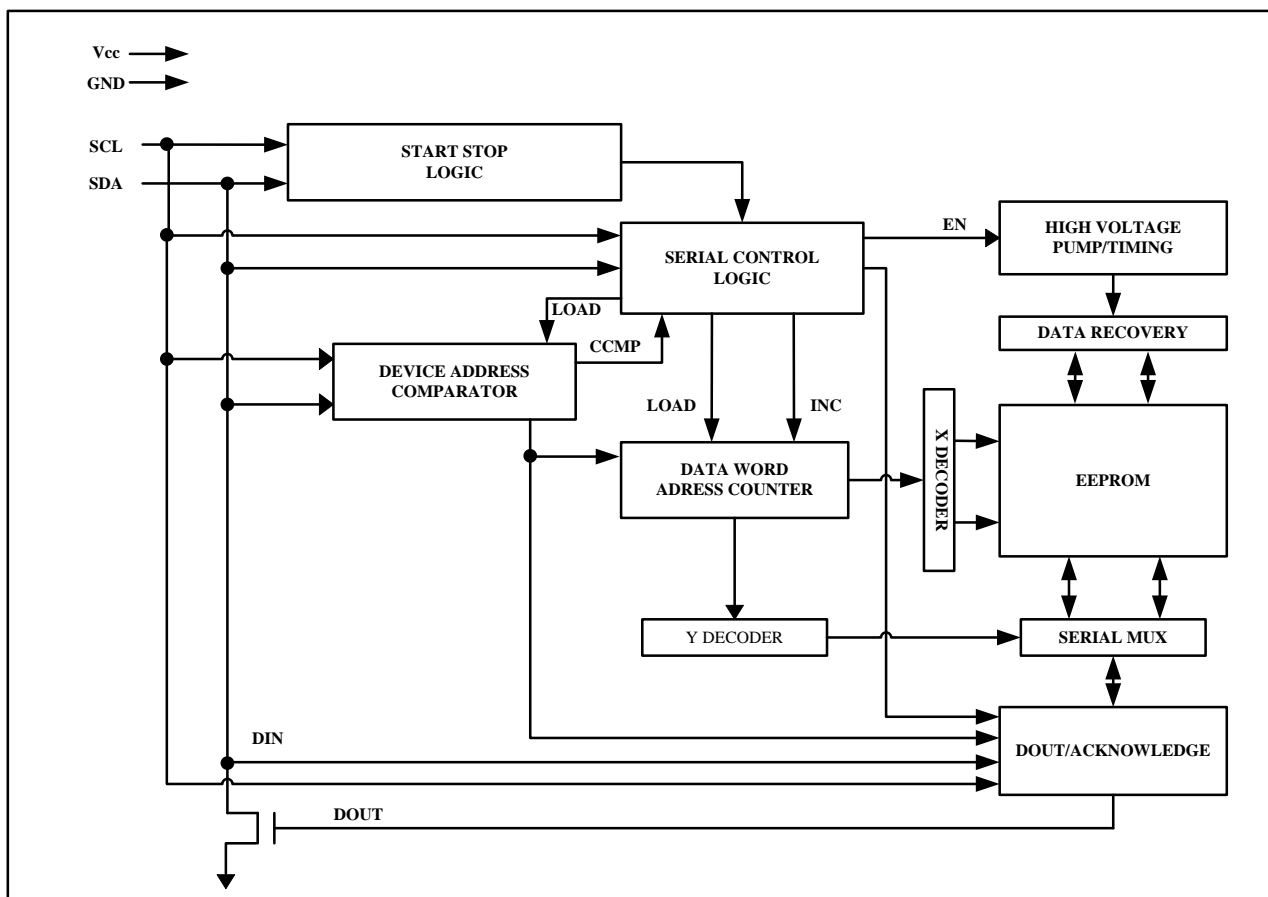
The BL24C128A provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 16,384 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The BL24C128A is available in space-saving WLCSP4 packages and is accessed via a two-wire serial interface. In addition, the BL24C128A is available in 1.7V (1.7V to 5.5V) version.

Pin Configuration



	Pin Name	Type	Functions
A1	Vcc	P	Power Supply
A2	SCL	I	Serial Clock Input
B1	SDA	I/O	Serial Data
B2	Vss	P	Ground

Block Diagram



SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

BL24C128A 128K bits (16,384×8)

Functional Description

1. Memory Organization

BL24C128A, 128K SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128K requires a 14-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The BL24C128A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

ILLEGAL INSTRUCTION : The EEPROM maybe sends a "0" to acknowledge that it has received any one of the following two instruction as write/read instructions.

1. Device address=1011 0000b.
2. Device address=1011 0001b

If device address=1011 0001b, next step need 9 cycles Clock to stop the instruction.

Figure 1. Data Validity

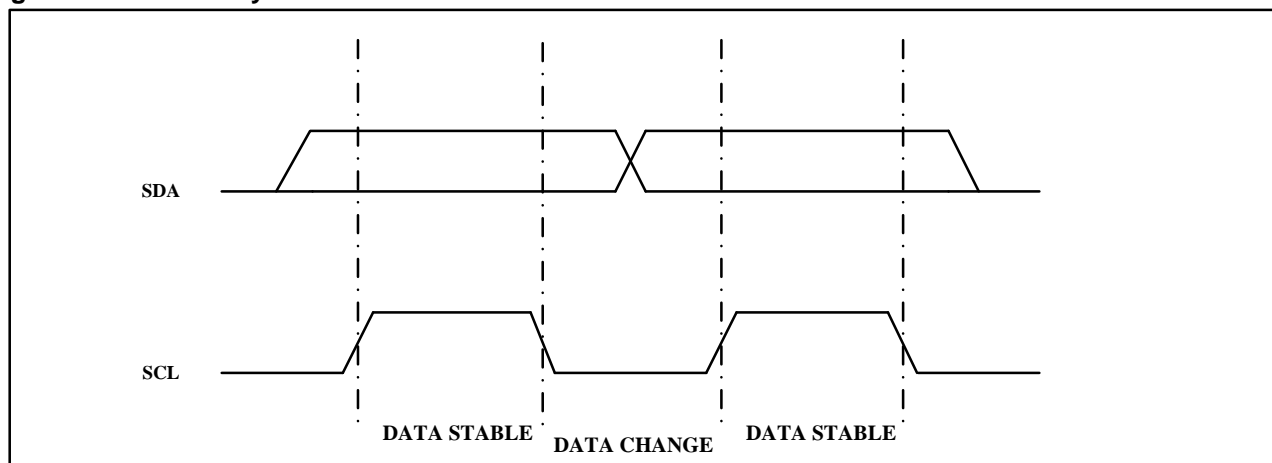


Figure 2. Start and Stop Definition

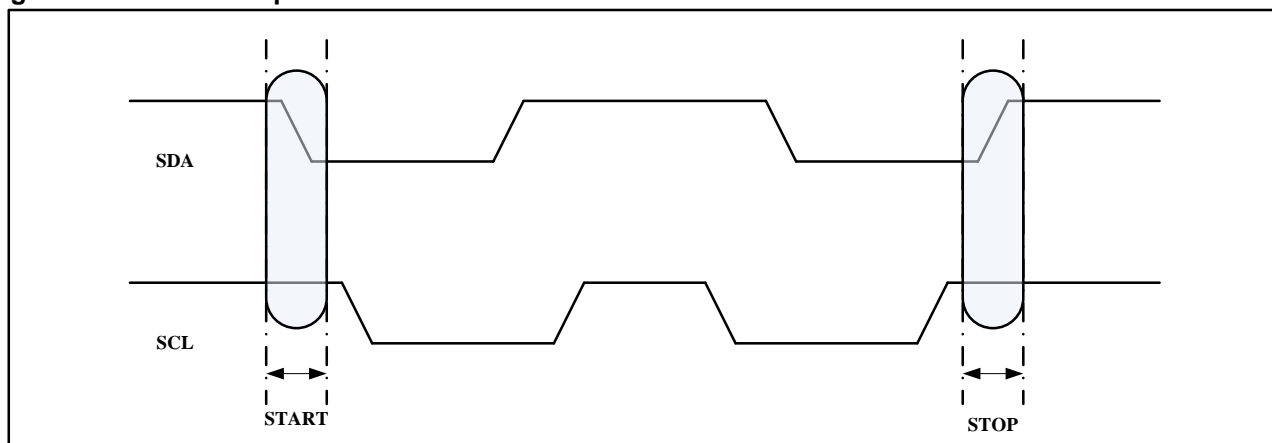
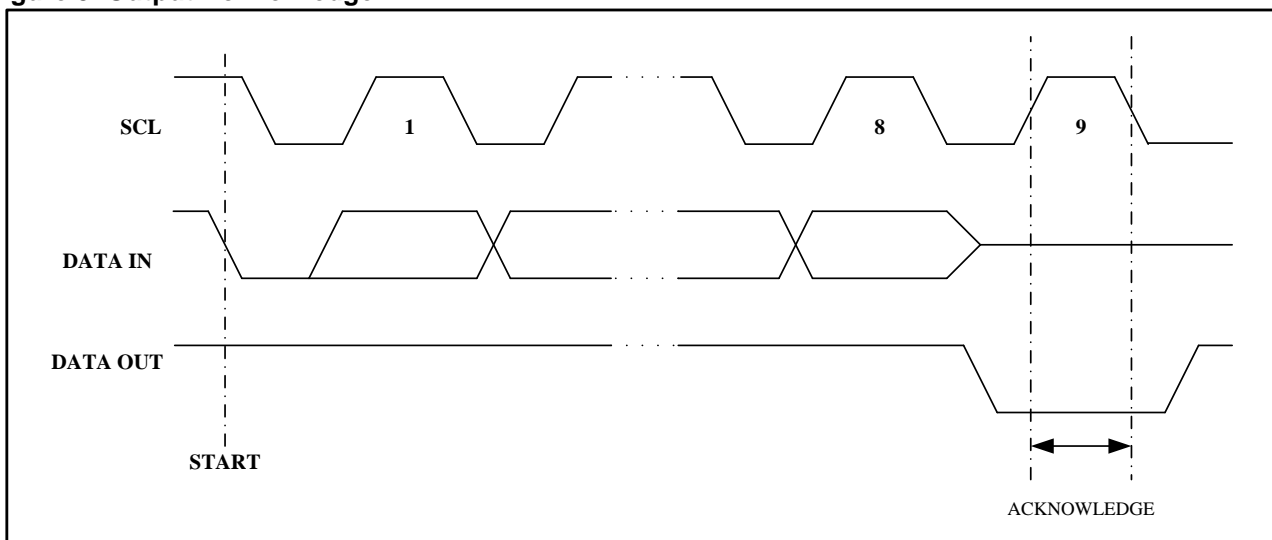


Figure 3. Output Acknowledge



3. Device Addressing

The 128K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The four most significant bits of the slave address are fixed (1010).

The next three bits are default to 0.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

PAGE WRITE: The 128K EEPROM is capable of an 64-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the

BL24C128A 128K bits (16,384×8)

read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

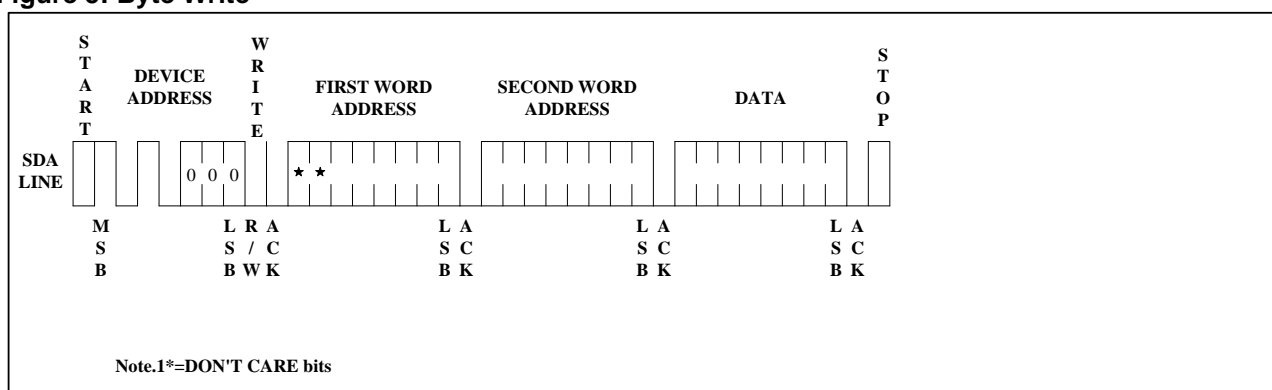
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

Figure 4: Device Address

MSB						LSB	
1	0	1	0	0	0	0	R/W

Figure 5: Byte Write



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Figure 6: Page Write

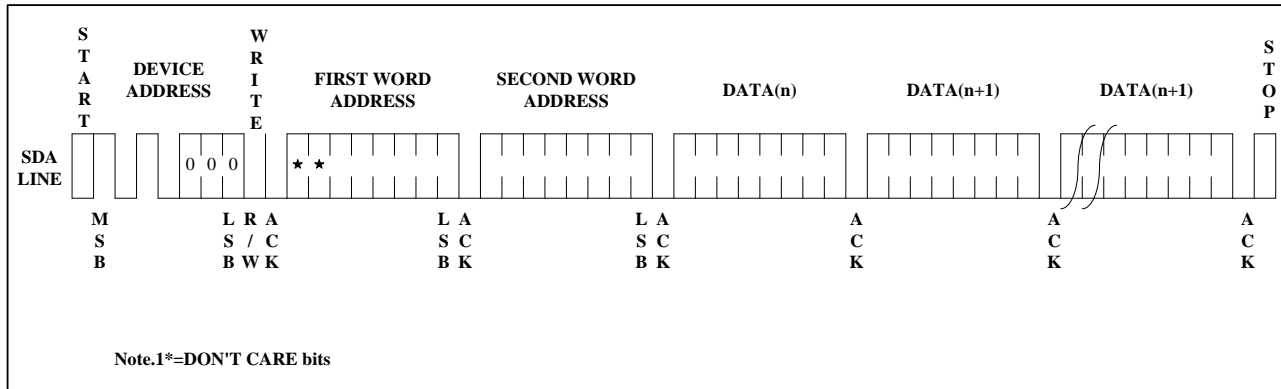


Figure 7: Current Address Read

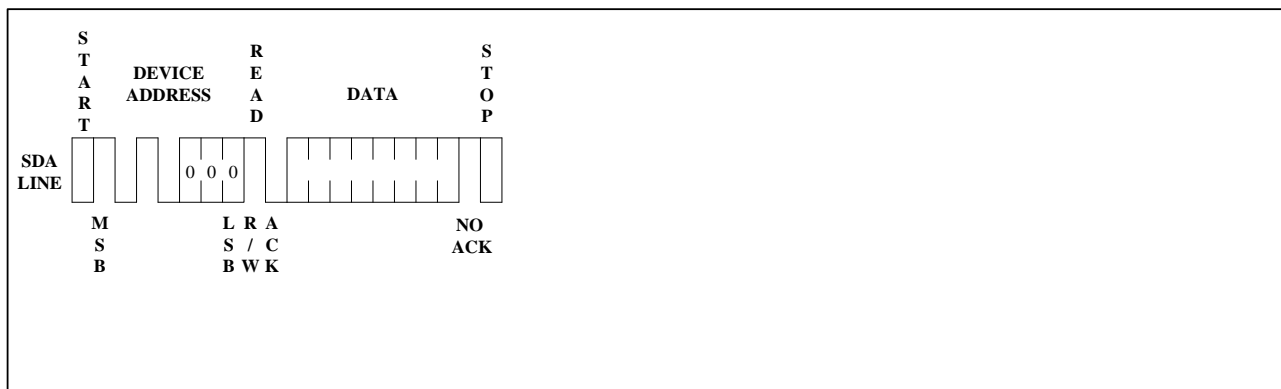


Figure 8: Random Read

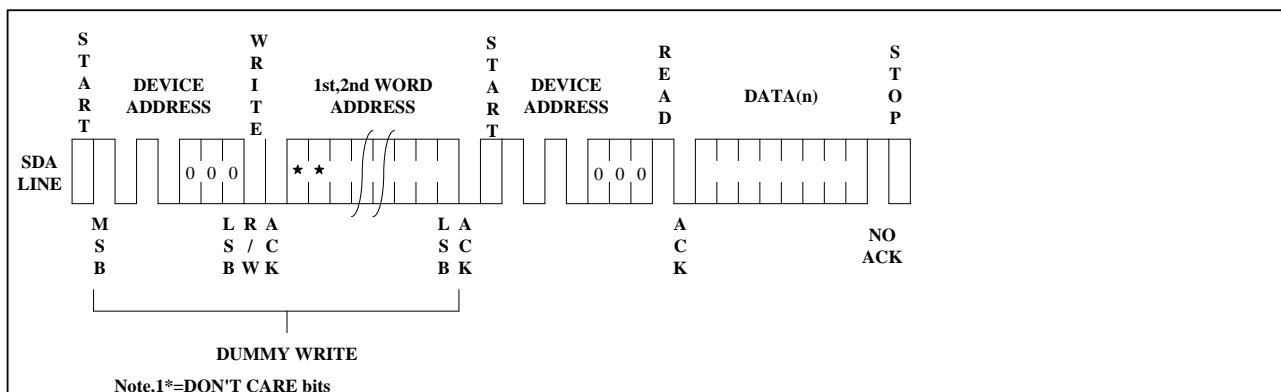
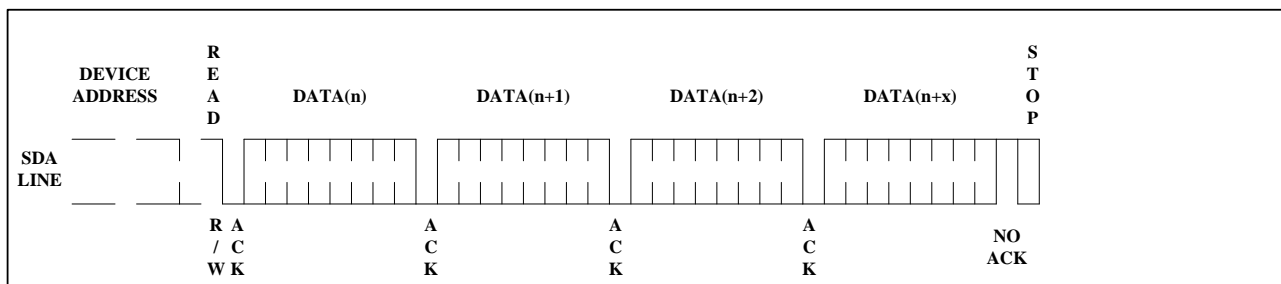


Figure 9: Sequential Read



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Electrical Characteristics

Absolute Maximum Stress Ratings :

- DC Supply Voltage-0.3V to +6.5V
- Input / Output Voltage.GND-0.3V to VCC+0.3V
- Operating Ambient Temperature.....-40℃ to +85℃
- Storage Temperature-65℃ to +150℃

● Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

BL24C128A 128K bits (16,384×8)**DC Electrical Characteristics**

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC = +1.7V to +5.5V
(unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V _{CC1}	1.7	-	5.5	V	-
Supply Voltage	V _{CC2}	2.5	-	5.5	V	-
Supply Voltage	V _{CC3}	2.7	-	5.5	V	-
Supply Voltage	V _{CC4}	4.5	-	5.5	V	-
Supply Current VCC=5.0V	I _{CC1}	-	0.4	1.0	mA	READ at 400KHZ
Supply Current VCC=5.0V	I _{CC2}	-	2.0	3.0	mA	WRITE at 400KHZ
Supply Current VCC=1.7V	I _{SB1}	-	0.6	1.0	μA	V _{IN} =V _{CC} or V _{SS}
Supply Current VCC=2.5V	I _{SB2}	-	1.0	2.0	μA	V _{IN} =V _{CC} or V _{SS}
Supply Current VCC=2.7V	I _{SB3}	-	1.0	2.0	μA	V _{IN} =V _{CC} or V _{SS}
Supply Current VCC=5.0V	I _{SB4}	-	2.0	5.0	μA	V _{IN} =V _{CC} or V _{SS}
Input Leakage Current	I _{L1}	-	0.10	3.0	μA	V _{IN} =V _{CC} or V _{SS}
Output Leakage Current	I _{LO}	-	0.05	3.0	μA	V _{OUT} =V _{CC} or V _{SS}
Input Low Level	V _{IL1}	-0.3	-	V _{CC} ×0.3	V	V _{CC} =1.8V to 5.5V
Input High Level	V _{IH1}	V _{CC} ×0.7	-	V _{CC} +0.3	V	V _{CC} =1.8V to 5.5V
Input Low Level	V _{IL2}	-0.3	-	V _{CC} ×0.2	V	V _{CC} =1.7V
Input High Level	V _{IH2}	V _{CC} ×0.7	-	V _{CC} +0.3	V	V _{CC} =1.7V
Output Low Level VCC=5.0V	V _{OL3}	-	-	0.4	V	I _{OL} =3.0mA
Output Low Level VCC=3.0V	V _{OL2}	-	-	0.4	V	I _{OL} =2.1mA
Output Low Level VCC=1.7V	V _{OL1}	-	-	0.2	V	I _{OL} =0.15mA

Pin Capacitance

Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	C _{I/O}	-	-	8	pF	V _{IO} =0V
Input Capacitance(A0,A1,A2,SCL)	C _{IN}	-	-	6	pF	V _{IN} =0V

BL24C128A 128K bits (16,384×8)**AC Electrical Characteristics**

Applicable over recommended operating range from TA = -40°C to +85°C, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.7V ≤ VCC < 2.5V			2.5V ≤ VCC < 5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	f _{SCL}	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	t _{LOW}	1.2	-	-	0.6	-	-	μs
Clock Pulse Width High	t _{HIGH}	0.6	-	-	0.4	-	-	μs
Noise Suppression Time	t _I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t _{AA}	0.1	-	0.9	0.05	-	0.9	μs
Time the bus must be free before a new transmission can start	t _{BUF}	1.2	-	-	0.5	-	-	μs
Start Hold Time	t _{HD:STA}	0.6	-	-	0.25	-	-	μs
Start Setup Time	t _{SU:DAT}	0.6	-	-	0.25	-	-	μs
Data In Hold Time	t _{HD:DAT}	0	-	-	0	-	-	μs
Data in Setup Time	t _{SU:DAT}	100	-	-	100	-	-	ns
Input Rise Time(1)	t _R	-	-	0.3	-	-	0.3	μs
Input Fall Time(1)	t _F	-	-	300	-	-	300	μs
Stop Setup Time	t _{SU:STO}	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t _{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t _{WR}	-	3.3	5	-	3.3	5	ms
5.0V,25°C,Byte Mode(1)	Endurance	1M	-	-	-	-	-	Write Cycle

Note:

1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to VCC): 1.3 k (2.5V, 5V), 10 k (1.7V) Input pulse voltages: 0.3 VCC to 0.7 VCC

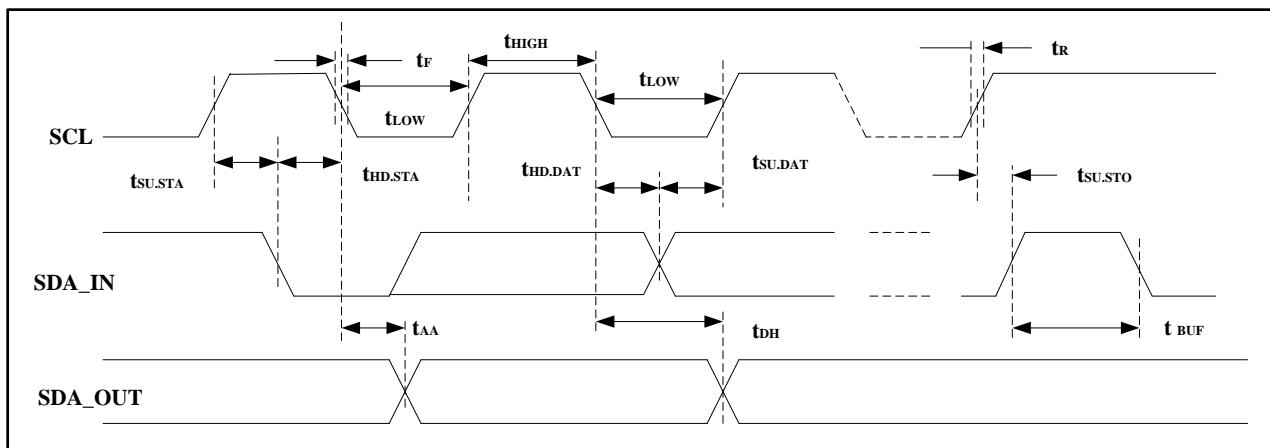
Input rise and fall time: 50 ns

Input and output timing reference voltages: 0.5 VCC

The value of RL should be concerned according to the actual loading on the user's system.

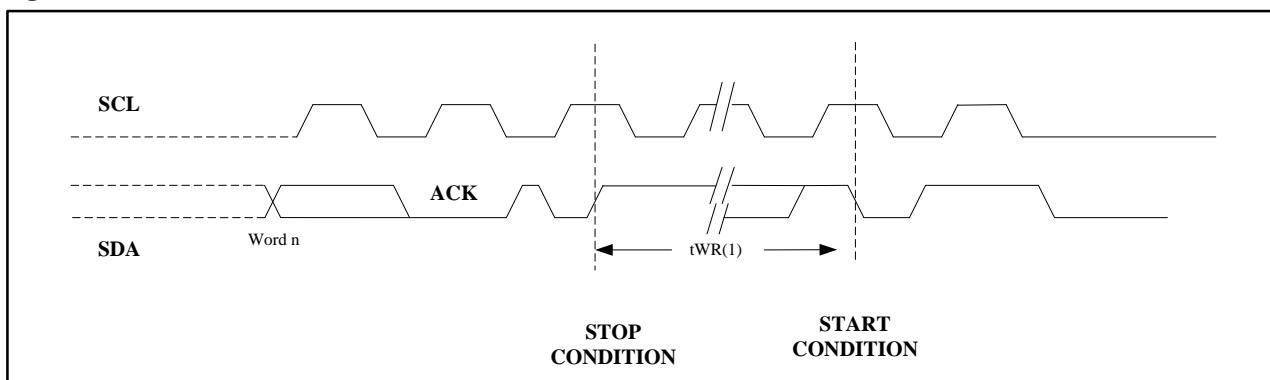
Bus Timing

Figure 10: SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 11: SCL: Serial Clock, SDA: Serial Data I/O



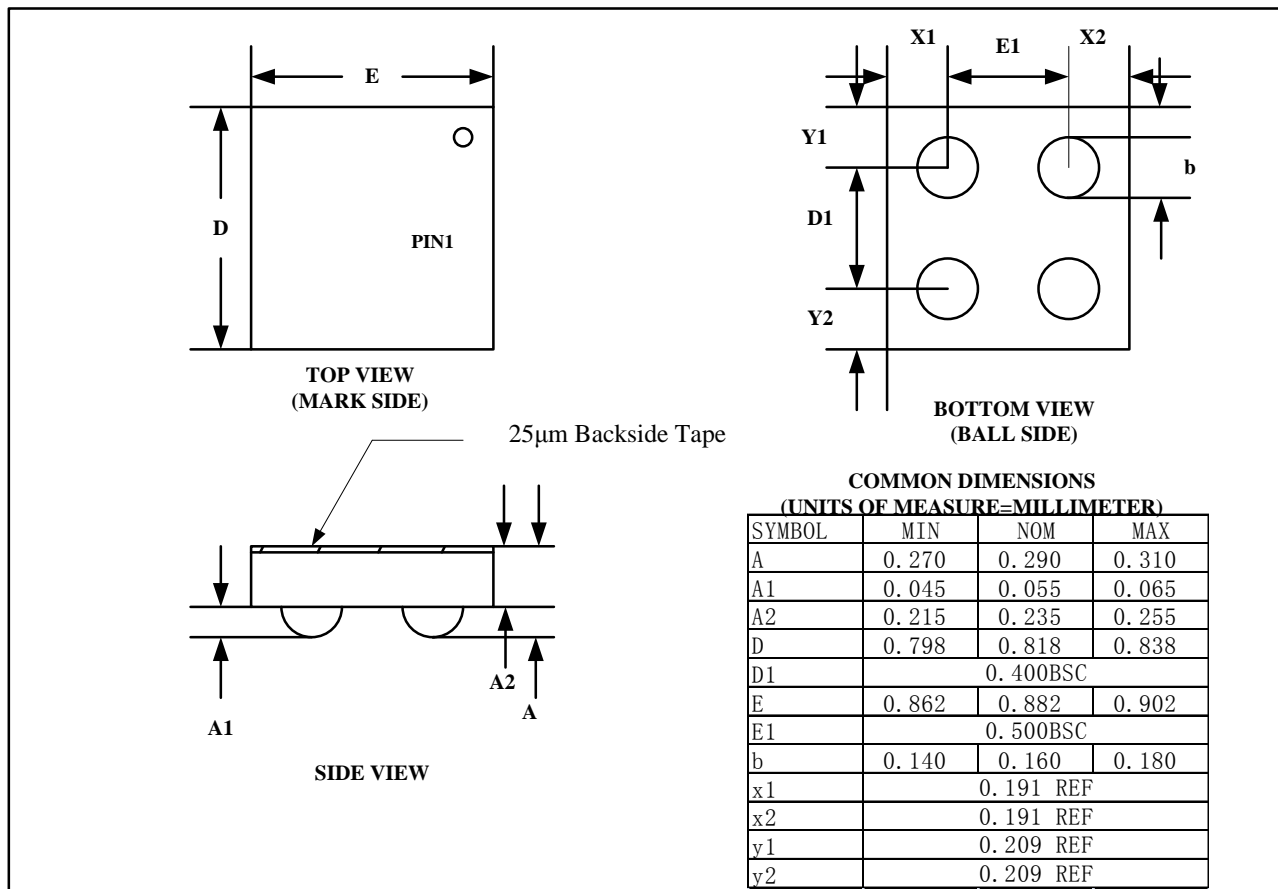
Note:

The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

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Package Information

WLCSP



Notes:

All wafer orientation notch down

Ordering Information

BL24C128A 1 2

Code	Description
1	Package type CS: WLCSP-4
2	Packing type R: Tape and Reel