1/6.5-Inch 1.2 Mega Pixel Image Sensor SP1628

Specification

Version Commercial 1.6

2013.01.23

SuperPix Micro Technology Co., Ltd

1/6.5-Inch 1.2 Mega Pixel Image Sensor Part Number SP1628

SuperPix® SP1628 is a 1/6.5 inch 1.2 mega pixels image sensor loaded with supreme sensor and ISP features, in terms of advanced 1.75um pixel structure which is a significant role for domestic pixel technology, and refined image signal processor delivering crystalline image quality and plenty of new functions. The SP1628 is a prominent representative of the 2nd generation CMOS image sensor technology and 1.75um pixel architecture based on SuperPix®'s proprietary designs, which has been proved as a reliable and efficient design and been embedded in variant Superpix® products. The integrated ISP features all standard image quality controls and a host of processing functions, performing 720P high definition images. Further more, with improved 50Hz/60Hz flicker detection function and MIPI interface SP1628 can deliver excellent images efficiently, and is a reliable choice for next generation camera for mobile handset, smart phone and tablet.

Functionalities

- CMOS Image Sensor
- Image Signal Processor

Applications

- Tablet
- Mobile Phone
- PC Camera
- Notebook Camera
- Toys

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Overview

General Description

SuperPix® SP1628 is a 1/6.5 inch 1.2 mega pixels image sensor loaded with supreme sensor and ISP features, in terms of advanced 1.75um pixel structure which is a significant role for domestic pixel technology, and refined image signal processor delivering crystalline image quality and plenty of new functions. The SP1628 is a prominent representative of the 2nd generation CMOS image sensor technology and 1.75um pixel architecture based on SuperPix®'s proprietary designs, which has been proved as a reliable and efficient design and been embedded in variant Superpix® products. The integrated ISP features all standard image quality controls and a host of processing functions, performing 720P high definition images. Further more, with improved 50Hz/60Hz flicker detection function and MIPI interface SP1628 can deliver excellent images efficiently, and is a reliable choice for next generation camera for mobile handset, smart phone and tablet.

Plenty of advanced features enable the SP1628 to become the best-in-class 1.2 mega CMOS sensor. The processing functions of SP1628 include all standard and advanced functions, for instance, advanced auto white balance, refined image sharpen and de-noise function, bad pixel calibration based on improved algorithm, advanced auto exposure control that supports an exposure time less than that of one row, which can avoid the overexposure phenomenon, and so forth. Moreover, SP1628 supports high frame speed up to 30fps at 1280 x 720 (720P) resolution and 37fps at 640 x 480 (VGA) resolution transferred over a one lane MIPI interface - Mobile Industry Processor Interface – or a traditional high speed parallel interface. The MIPI interface will perform excellent with rapid data transfer, increasing reliability, and reducing power consumption.

An overview of the SP1628 Image Sensor features and functions will be given below.

Function Diagram

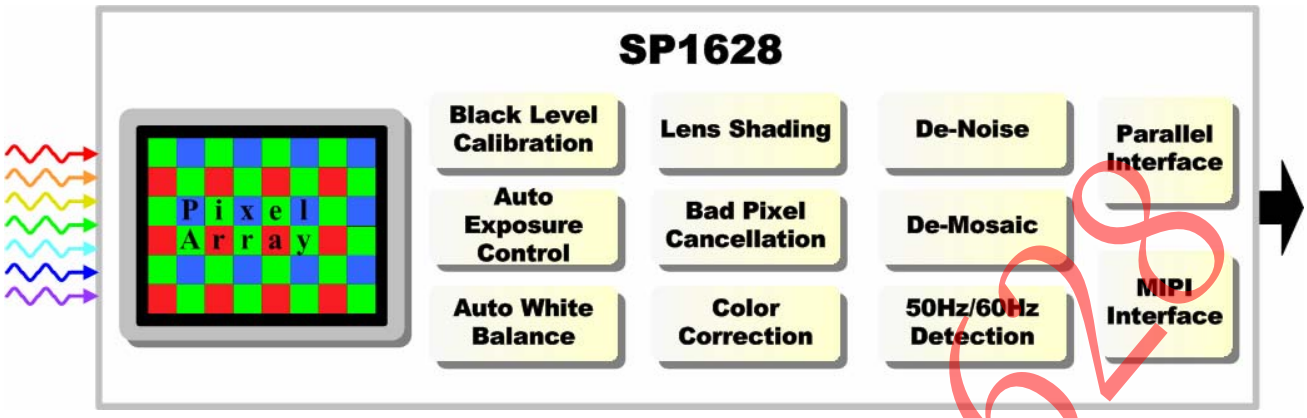


Figure 1 Function Diagram

Typical Application List

- Tablet
- Mobile Phone
- PC Camera
- Notebook Camera
- Toys

Typical Application Diagram

Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	1280 x 960
Pixel Size	1.75um x 1.75umSquare Pixel
Lens Size	1/6.5 inch
Color Filter	Primary Color Filter Bayer Arrangement
Power Supply	I/O 1.7V ~ 3.0V
	Analog 2.6V ~ 3.0V
Power consumption	Active 120mA
	Standby 50uA
Data format	Raw8
	Raw10
	YUV422
	RGB565
Output Formats	MIPI CSI-2 1lane
	8bit Parallel
Input Clock	10 – 30 MHz
Max. Frame Rate	23fps@XVGA Mode – 1280 x 960
	30fps@720P Mode – 1280 x 720
	37fps@VGA Mode – 640 x 480
Shutter	Rolling Shutter
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	COB / TSV

Table 1 Key Performance Parameters

Features List

- Support XVGA (1.2Mega, 1280x960) resolution
- Support 720P (0.9Mega, 1280x720) resolution
- Support VGA (0.3Mega, 640x480) resolution
- Advanced 1.75um x 1.75um pixel architecture
- Embedded image preprocessor functionality

  - Automatic Black Level Calibration

  - Automatic White Balance

  - Automatic Exposure Control

  - Gamma Correction

  - Lens Shading Compensation

  - De-mosaic Function

  - De-noise Function

  - Color Correction Function

  - Bad Pixel Correction

  - Special Effect: Sepia, Monochrome, Emboss, Sketch, Neon, Grey, Solarize, Posteraize, Enchase
- I²C bus controlling registers inside chip
- Support 2 x 2 binning function
- Support auto 50Hz/60Hz flicker detection
- Support strobe signal in order to control flash lamp
- Support high speed parallel output interface
- Support MIPI (CSI-2) interface

Function Description

Pixel Array Structure

The SP1628 pixel array is configured as of 1316 columns by 1042 rows, shown below. There are 1280 columns by 960 rows of optically active pixels.

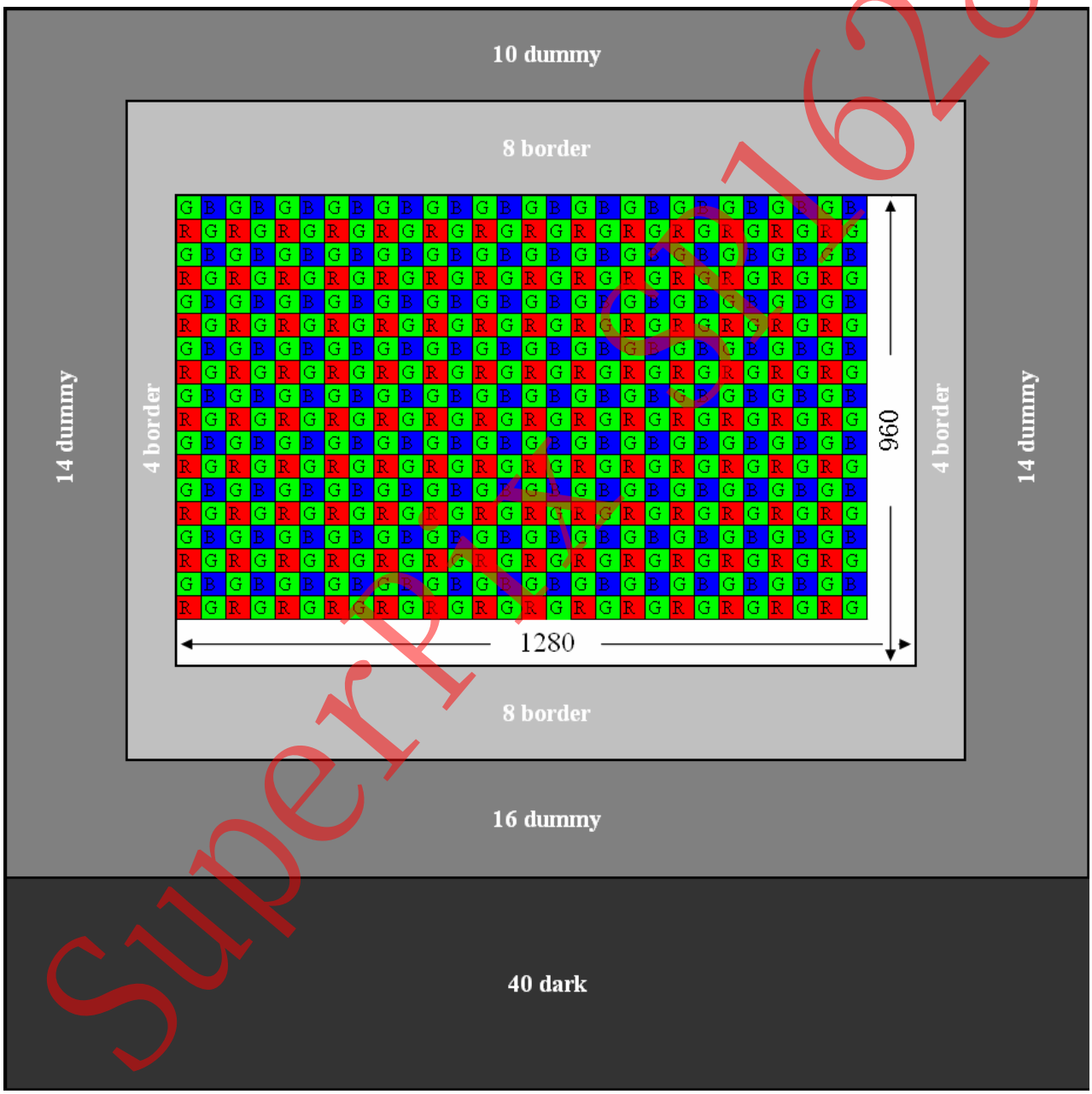


Figure 3 Pixel Floor Plan

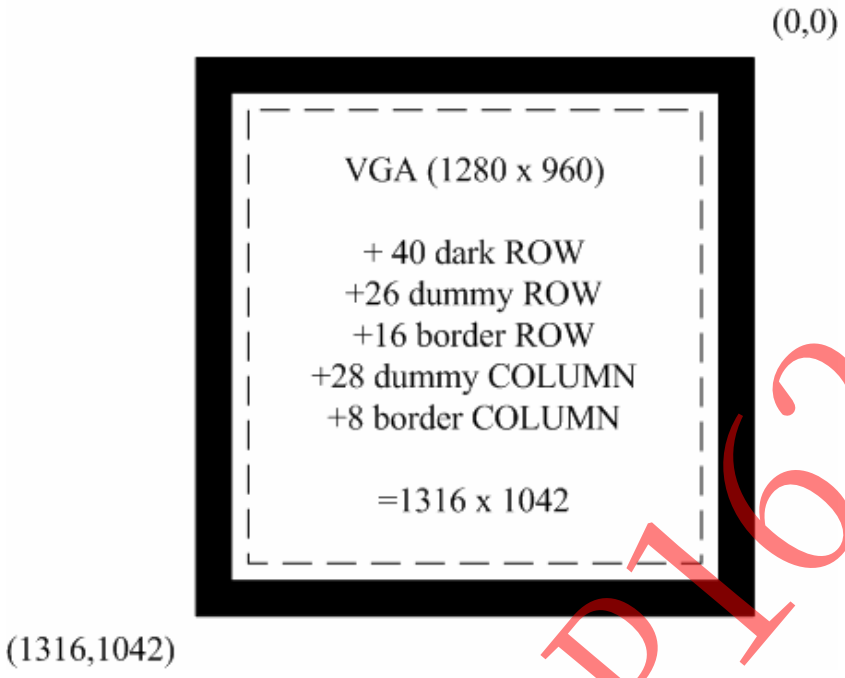


Figure 4 Sensor Pixel Description

Image Sensor Function

- Mirror and Flip
- Windowing
- Test Pattern
- Automatic Black Level Calibration
- Automatic White Balance
- Automatic Exposure Control
- Automatic Black Level Correction
- Gamma Correction
- Lens Shading Compensation
- De-mosaic Function
- De-noise Function
- Color Correction Function
- Bad Pixel Correction
- RGB to YUV Conversion
- YUV to RGB Conversion
- Special Effect
- 50Hz/60Hz Flicker Detection
- MIPI Interface
- Parallel Interface

Mirror and Flip

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.

Original Mirrored Flipped Mirrored and Flipped

Figure 5 Mirror and Flip

Windowing

The embedded windowing function extract an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By property setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Automatic Black Level Calibration

The pixel array contains several optically black lines, which can be seen at the pixel array structure section. These lines are used to provide the data for black level calibration and further correction.

Automatic White Balance

Auto white balance unit is help to remove the unrealistic color from the image automatically by referencing the white balance pre-gain. With auto white balance unit, the still / video camera system can determine the color temperature of the light and automatically adjust for the color temperature.

Automatic Exposure Control

After Gamma unit, the Y value, calculated by R, G, and B values, used to evaluate the luminance and exposure time, digital gain, analog gain are adjusted by this block to get the right luminance for the image.

Gamma Correction

The main purposed of the Gamma correction function is to compensate the characteristics of the sensor. According to de gamma curve, the pixel values can be converted in order to compensate the sensor output on different light strength conditions.

Lens Shading Compensation

Lens imperfection can be eliminated by lens shading compensation. It starts with the first pixel of a frame when the lens shading compensation unit is enabled, and correcting each pixel with its gain values.

The lens shading correction is based on one or more reference frames which have to be captured under dedicated light conditions and a dedicated position of the sensor. The pixels of the captured frame are then evaluated by software and the calculated parameters for lens shading correction are stored in different tables. It is also possible to use different lens shading correction parameters for different environment conditions. Therefore additional reference frames for the different conditions are to be captured and evaluated. The calculated parameters including sector settings can be stored in multiple tables.

De-mosaic Function

De-mosaic function is to convert the raw data to RGB image data. The algorithm is a digital image process used to interpolate a complete image from the partial raw data received form the color filter in form of a matrix of colored pixels. Each raw pixel data is converted to RGB value using an edge-sensitive color interpolation algorithm.

De-noise Function

The de-noise function can reduce the noise existing on edges markedly and smooth the shades.

Color Correction Function

The color correction function is including various color profiles that are used for color representation improvement. The function works by making decision based on scene brightness and illumination type.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit. A bad pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

RGB to YUV Conversion

It is used to convert the RGB color space to YUV color space so that the following image processing can be done in the YUV color space.

YUV to RGB Conversion

This block converts YUV to RGB so that the ISP can output RGB directly.

Special Effect

A set of image special effect is supported which includes monochrome, negative, sepia and emboss.

50Hz/60Hz Flicker Detection

To avoid image flickering under a periodic light source, the flicker detection function is to detect and adjust the flicker according to the period of the light source.

AC powered light sources usually have a frequency of 50Hz or 60Hz. When the sensor integration time is not an integer multiple to the light frequency, the image will flicker, and flicker sometimes is shown in terms of horizontal banding. With the flicker detection, the flicker detect the current light frequency automatically and eliminate the rolling horizontal banding (flicker) caused by the 50Hz/60Hz lighting.

Strobe Control

To achieve the plausible best image quality in low light conditions, the programmable strobe control function is integrated to control a strobe flash.

Strobe Signal

The strobe signal generated by SP1628 can be programmable, and SP1628 provide 3 different modes which will be illustrated below.

Strobe Mode 0 & 1

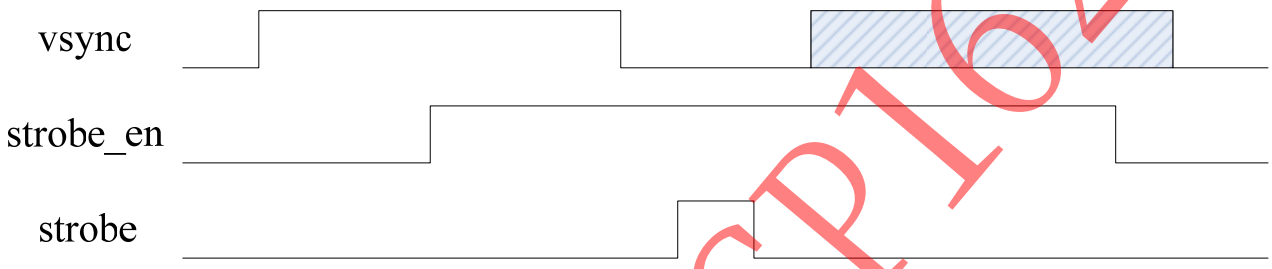


Figure 6 Strobe Mode 0 & 1

When the strobe signal is triggered in mode 0 or 1, the strobe signal will be launched at “vblank” level, the width of it can be chosen as 1 or 4, and the next frame – the one is colored shown at the figure above – then can be exposed accurately.

mode 0, 1 row width strobe
mode 1, 4 row width strobe

Strobe Mode 2

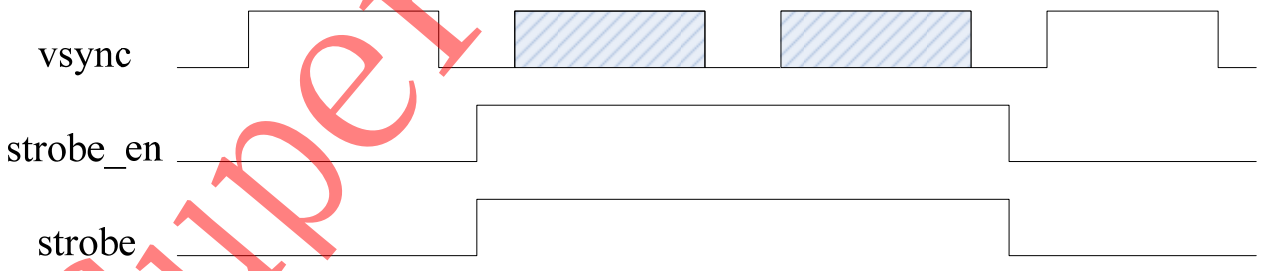


Figure 7 Strobe Mode 2

When the strobe signal is triggered in mode 2, the strobe signal will be launched immediately, and the next frame – the one is colored shown at the figure above – then can be exposed accurately.

Output Interface

- MIPI Interface
- Parallel Interface

Both MIPI data output interface and parallel data output interface integrated inside the sensor chip.

MIPI Interface

MIPI Interface – Mobile Industry Processor Interface is the most important data transport path for the next generation mobile phone, which defines standards for the interface between SP1628 modules of a mobile. The MIPI interface can support large data stream better than any other data interface. With it the sensor can provide more high definition images to the mobile phone.

MIPI interface provides one single uni-directional clock lane and one bi-directional data lane solution for communication links between components inside a mobile device. Data lane has full support for HS (uni-directional) and LP (bi-directional) data transfer mode.

Parallel Interface

Parallel Interface defines an interface between a peripheral device and a host processor. The parallel interface tends to be the output interface of most camera devices, and can be configured to operate as a camera interface. This sensor is built on the heritage and experience in the concept of high quality Superpix® traditional high speed parallel interface.

PLL and Clock Generator

The sensor contains a Phase Locked Loop (PLL) block, which generates all the necessary internal clocks from the external clock input.
The internal function block of the PLL is shown below.

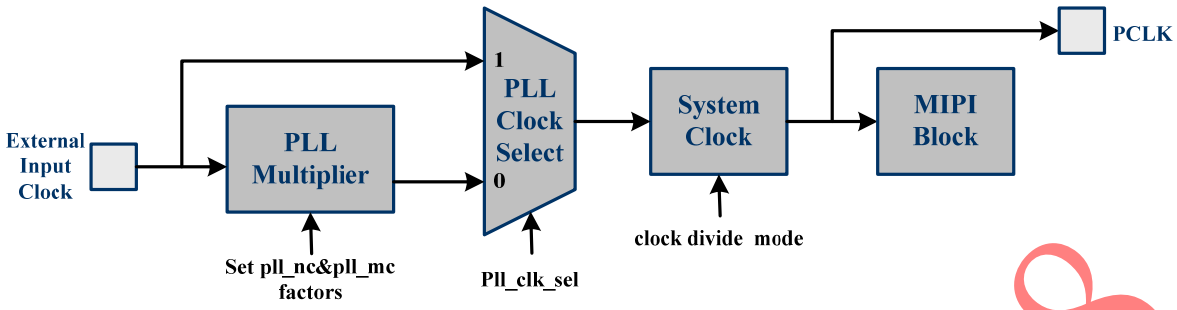


Figure 8 PLL Function Block

I²C Bus

Single WRITE and Single READ

A typical WRTIE or READ sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

SP1628 has 2 pairs of I^2C address, and which pair to be chosen is decided by the value of I^2C ID pad. When the value of I^2CID pin is 0, the write address is 78H, and the read address of that is 79H. When the I^2CID pin is 1, the write address is 7AH,

while the read address of that is 7BH.

Tow figures that is shown below will illustrate SP1628 single WRITE sequence and single READ sequence.

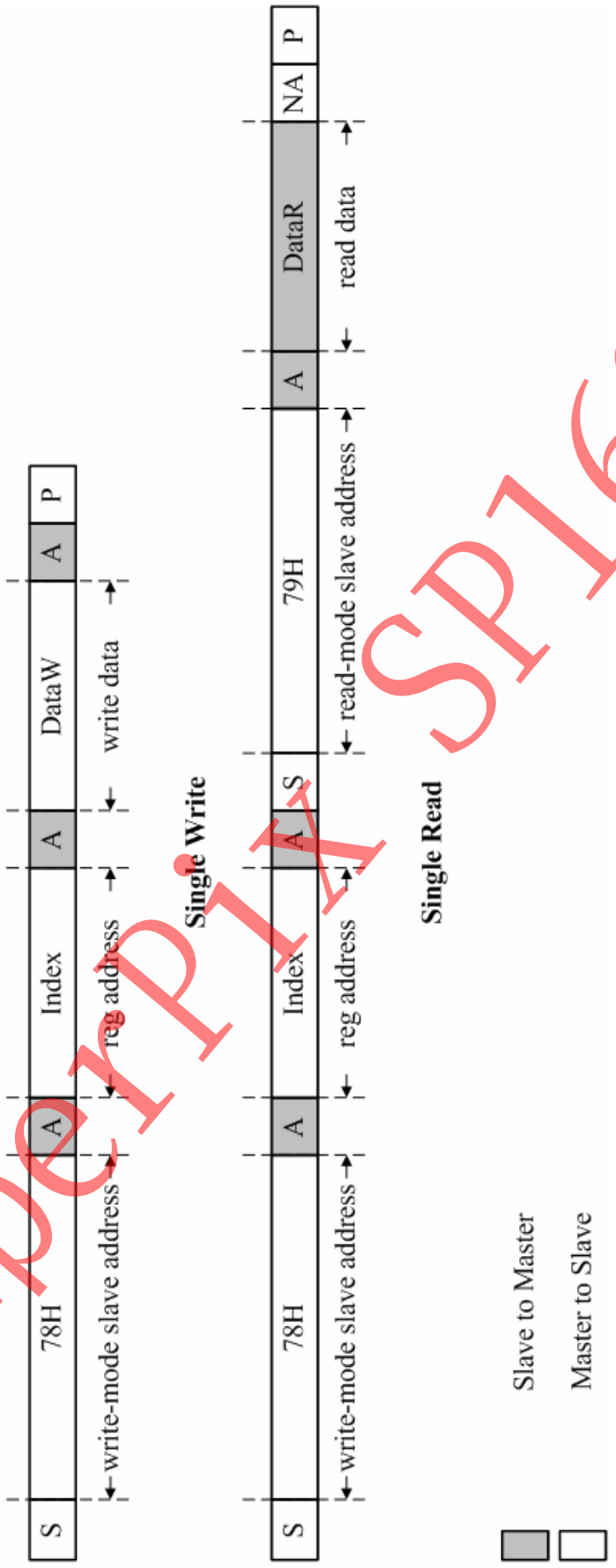


Figure 9 I²C Read & Write Description – I²CID Pin 0

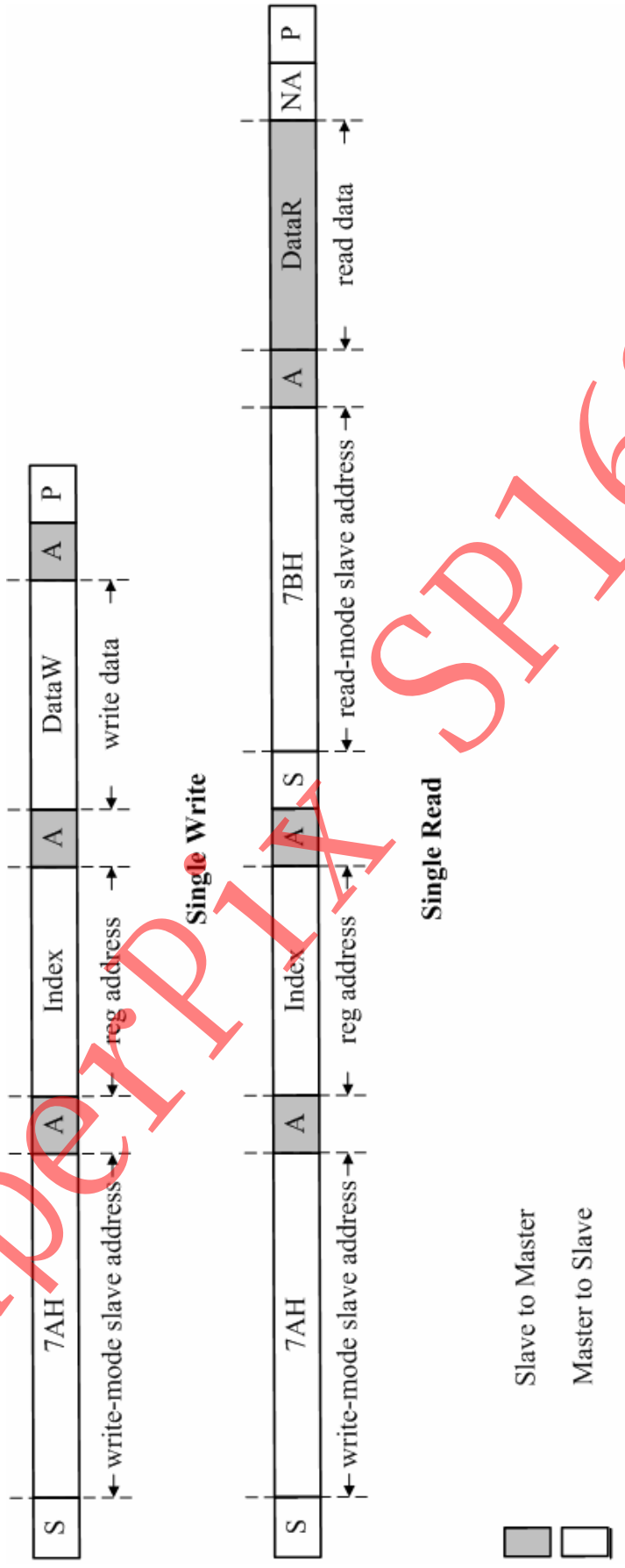


Figure 10 I²C Read & Write Description – I²CID Pin 1

Start/Stop Conditions

The serial bus will recognize logic 1 to logic 0 transition on the SDA pin while the SCLK pin is at logic 1 as the start condition. A logic 0 to logic 1 transition on the SDA pin while the SCLK pin is at logic 1 is interrupted as the stop condition.

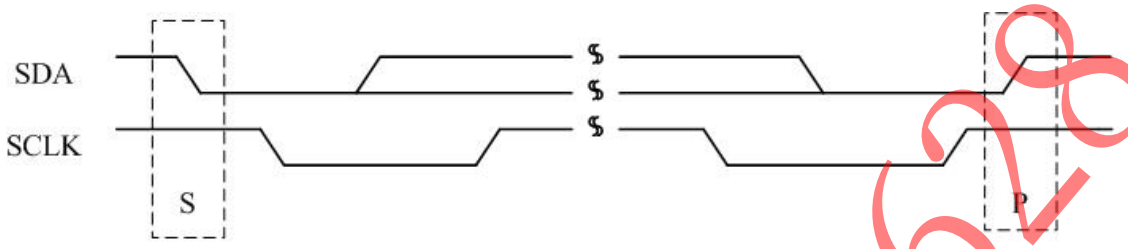


Figure 11 I²C Start & Stop Description

Acknowledge Bit

The SP1628 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

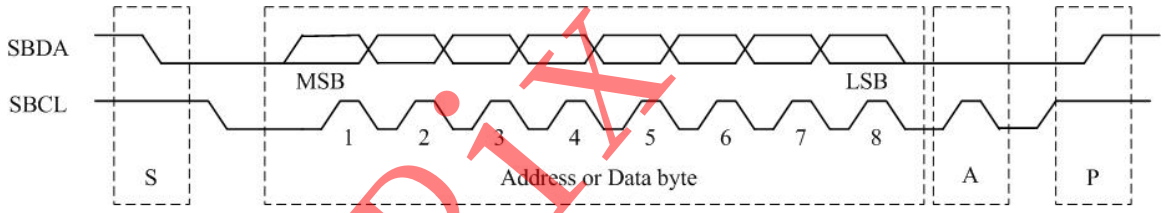


Figure 12 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

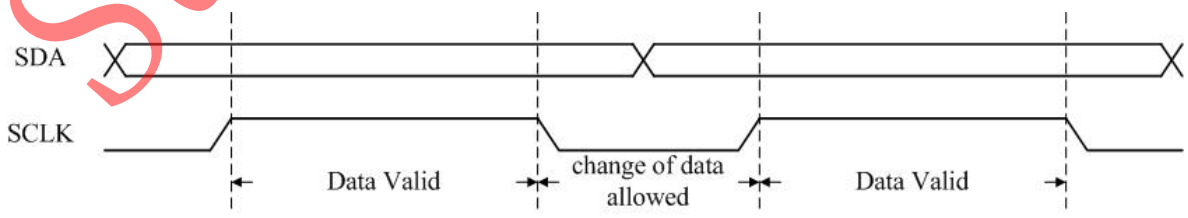


Figure 13 I²C Data Transport Description

Timing Parameter

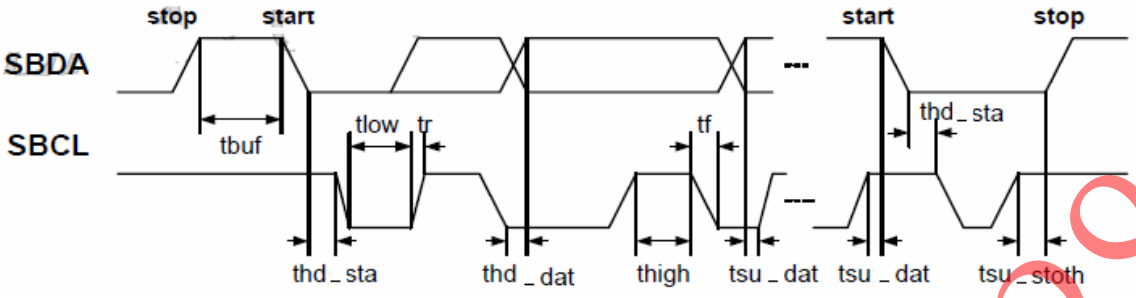


Figure 14 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Data Output Timing

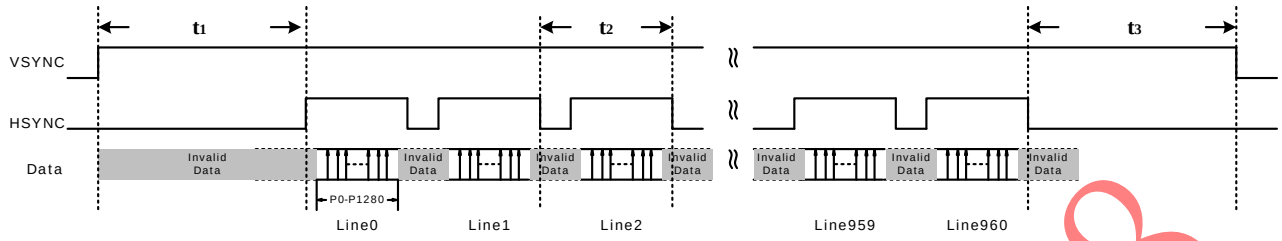


Figure 15 Data Output Timing

The relative registers are P1:0x5f and P1:0x2f, the details of the registers is described below.

Address	Register Name	Bits	Description	Default
P1:0x5f	row_add4_en, col_add4_en, vsync_pre_num	5~0	[5]: row_add4_en 1: Output more 4 rows after demosaic . 0: disable [4] : col_add4_en 1: output more 4 data every line after demosaic 0:disable [3:0]:vsync_pre_num t1 = (8-vsync_pre_num)*t2 (unit is pclk)	0x06
P1:0x2f	vs_dly_num_reg	7-0	[7] : vs_dly_en 1: vsync delay enable 0: disable [6:0]:vs_dly_reg t3 = 960+ vs_dly_reg*2 (unit is pclk) If enable row_add4_en function and window function t3 = 960+ vs_dly_reg*2 + (4-v_start)*t2 (v_start write 2 at least)	0x00

Electric Characteristics

DC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.7	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		1.2xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			1.2xVDDIO	V
T	Junction Temperature	-20	25	70	**°C**

Examination Item

No.	Reliability Items	Condition
1	Temp Cycle	-20°C ~ 70°C each 30 min, 24 cycles
2	High Temp. & Humidity storage	70°C / 80% / 72Hr
3	Low Temp. & Humidity storage	-20°C / 96Hr natural dry, for 3 hours
4	High Temp Operating	70°C / 80% / 72Hr / 2.8V other pins are active condition
5	Low Temp Operating	-20°C / 72Hr / 2.8V other pins are active condition
6	Drop Test	1.5m drop, 1 X 6 plane (Camera with 100g cradle)
7	Random Vibration	5~100HZ, 3 axis (X,Y,Z),15min/axis,swing :6mm

Power Sequence

Power Up Sequence

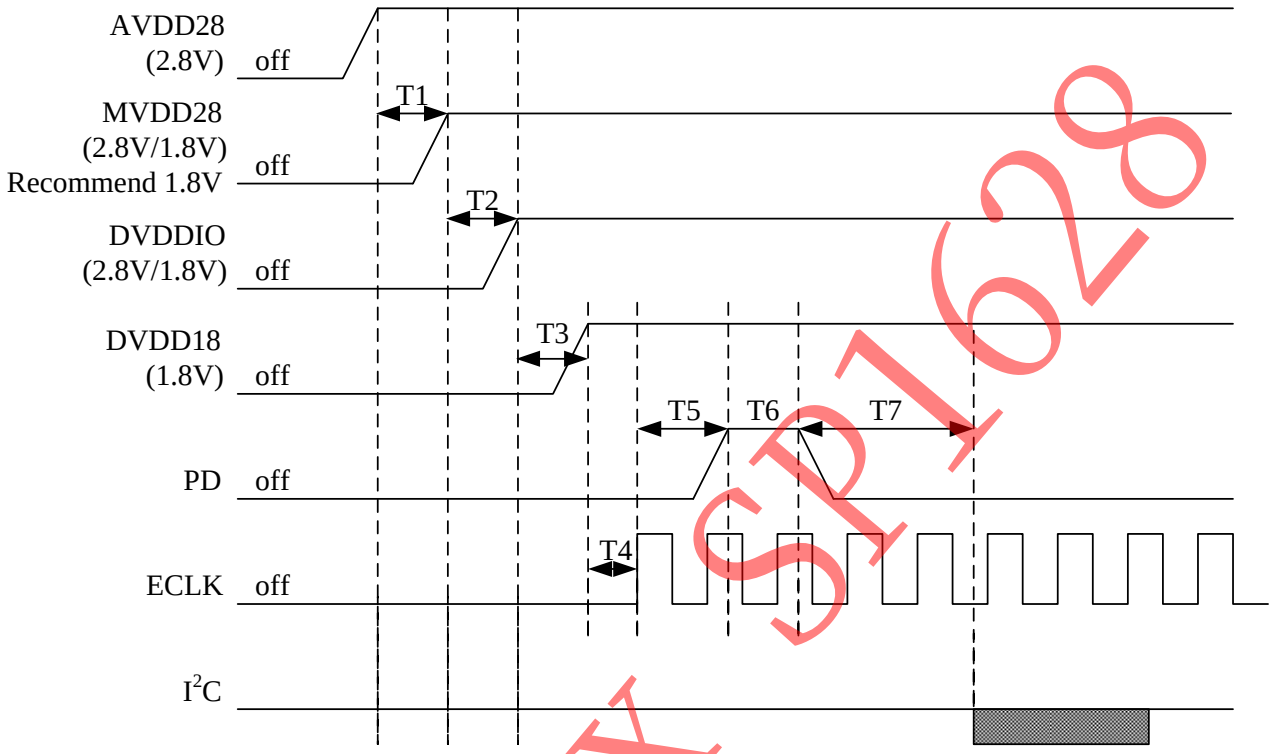


Figure 16 Power Up Sequence

Symbol	Description	Min.	Unit
T1	Time from AVDD28 to MVDD28	0	ms
T2	Time from MVDD28 to DVDDIO	0	ms
T3	Time from DVDDIO to DVDD18	0	ms
T4	Time from DVDD18 to clock plus input	0	ms
T5	Time from clock plus input to PD up edge	0	ms
T6	PD high plus time	100	ns
T7	Time from PD down edge to available I^2C	5	ms

Power Off Sequence

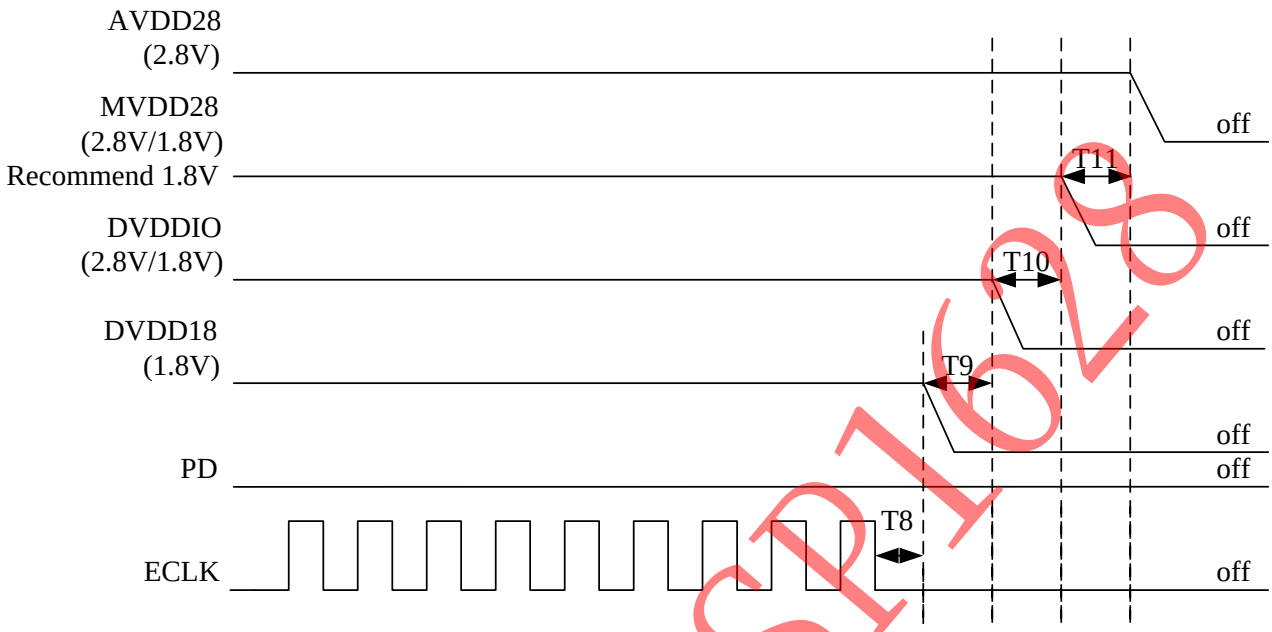


Figure 17 Power Down Sequence

Symbol	Description	Min.	Unit
T8	Time from clock plus stop to DVDD18	0	ms
T9	Time from DVDD18 to DVDDIO power down	0	ms
T10	Time from DVDDIO to MVDD28 power down	0	ms
T11	Time from MVDD28 to AVDD28 power down	0	ms

CRA Information

Field(%)	RIC(mm)	CRA
0	0	0
5	0.07	2.10955
10	0.14	4.1993
15	0.21	6.28435
20	0.28	8.3643
25	0.35	10.4331
30	0.42	12.46375
35	0.49	14.438
40	0.56	16.34115
45	0.63	18.13165
50	0.7	19.79655
55	0.77	21.30195
60	0.84	22.6338
65	0.91	23.7794
70	0.98	24.7182
75	1.05	25.46625
80	1.12	26.00885
85	1.19	26.361
90	1.26	26.5154
95	1.33	26.4812
100	1.4	26.3218

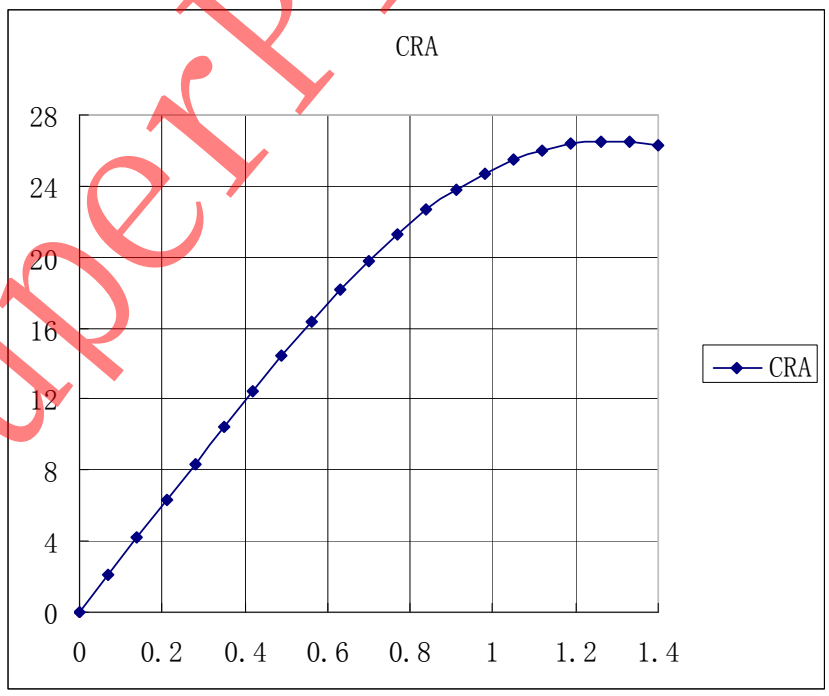
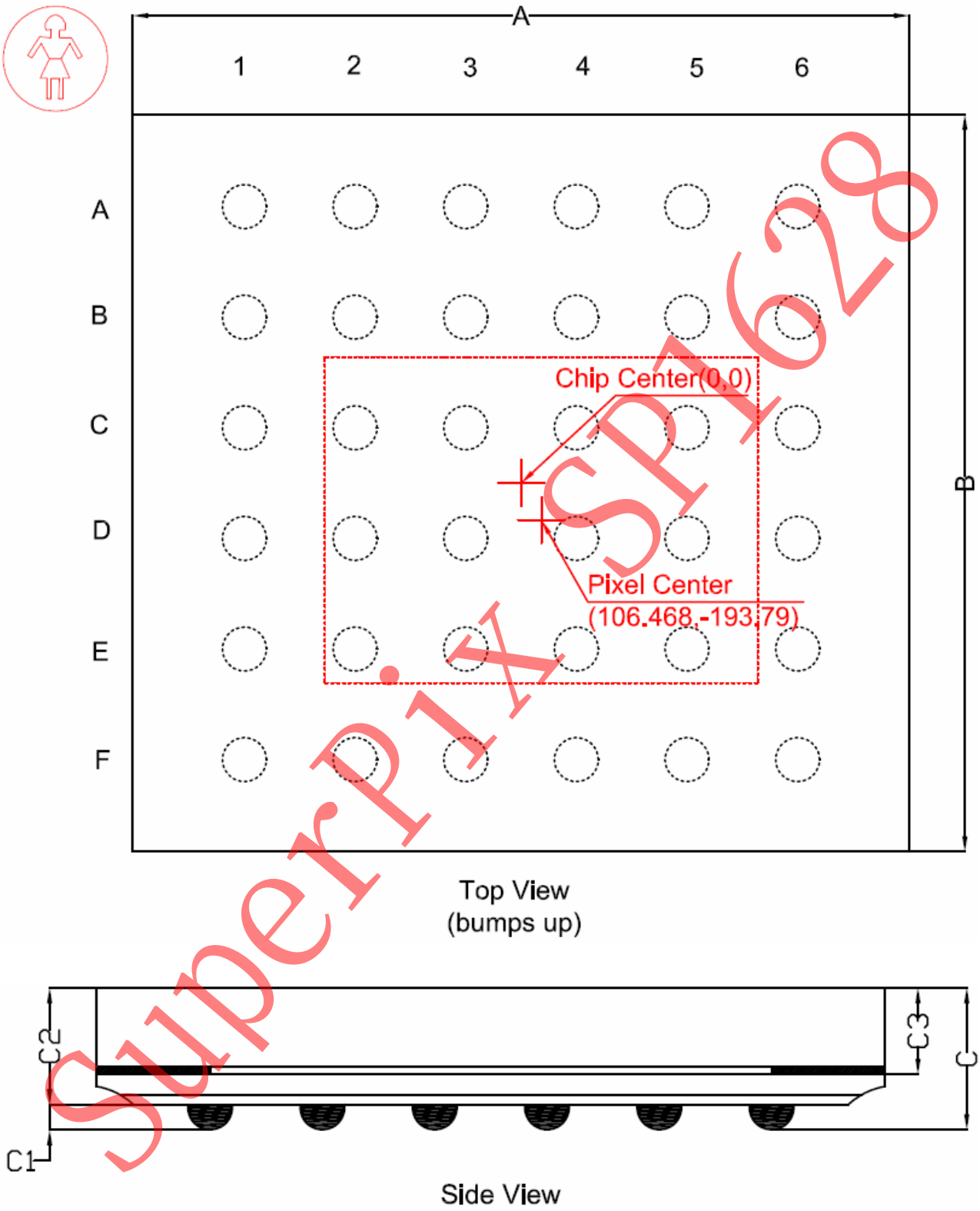
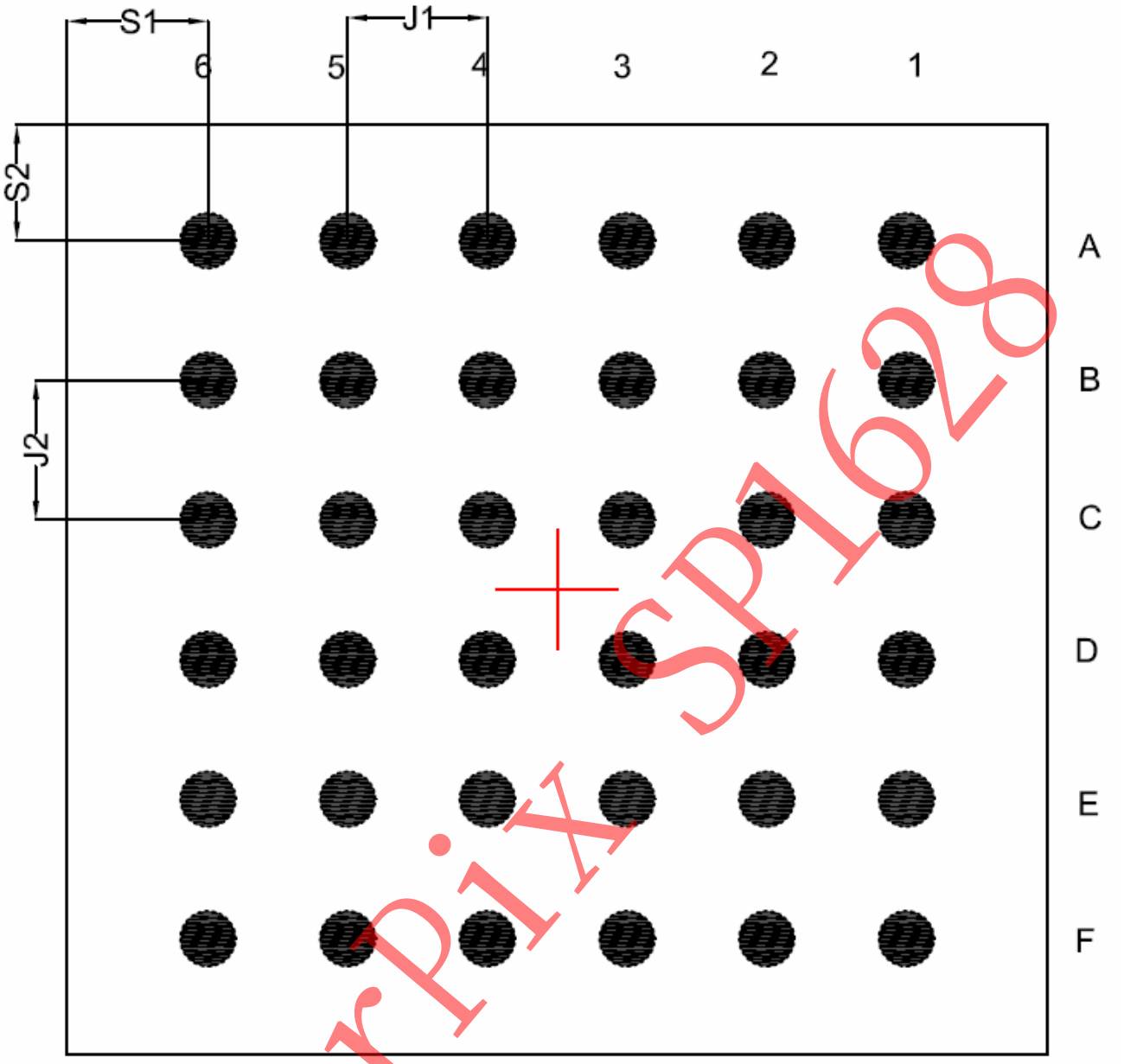


Figure 18 CRA Information

Package Information





Bottom View
(bumps up)

	1	2	3	4	5	6
A	I2CID	D3	D5	PCLK	DVDD28	DGND
B	SBCL	DVDD28	D4	D7	HSYNC	DVDD18
C	PD	SBDA	D2	D8	ECLK	AVDD28
D	OUTAM	OUTAP	STROBE	D6	D9	AGND28
E	MGND28	OUTCM	OUTCP	DGND	RSTB	DVDD15
F	AVDD28	MVDD28	MVDD15	AGND28	VSYNC	AVDD28

Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	4070	4045	4095
Package Body Dimension Y	B	3866	3841	3891
Package Height	C	730	670	790
Ball Height	C1	130	100	160
Package Body Thickness	C2	600	565	635
Thickness of glass surface to wafer	C3	445	425	465
Ball Diameter	D	230	200	260
Total Ball count	N	36	—	—
Pin pitch1 X axis	J1	580	—	—
Pin pitch Y axis	J2	580	—	—
Edge to Pin Center Distance along X	S1	585	555	615
Edge to Pin Center Distance along Y	S2	483	453	513

Table 2 Package Dimension

NO.	Pad Name	I/O	Description
A1	I2CID	I	I2C Slave address select
A2	D3	O	Pixel Array Output bit 3
A3	D5	O	Pixel Array Output bit 5
A4	PCLK	O	Pixel Output Clock
A5	DVDD28	DP	Digital Power 2.8V
A6	DGND	DG	Digital Ground
B1	SBCL	I	Slave I2C clock bus
B2	DVDD28	DP	Digital Power 2.8V
B3	D4	O	Pixel Array Output bit 4
B4	D7	O	Pixel Array Output bit 7
B5	HSYNC	O	Horizontal Sync Signal
B6	DVDD18	DP	Digital Power 1.8V
C1	PD	I	Power down, "0" normal
C2	SBDA	I/O	Slave Tri-state I2C data bus
C3	D2	O	Pixel Array Output bit 2
C4	D8	O	Pixel Array Output bit 8
C5	ECLK	I	Input system clock
C6	AVDD28	AP	Analog Power 2.8V
D1	OUTAM	O	MIPI data output -
D2	OUTAP	O	MIPI data output +
D3	STROBE	O	Strobe Signal
D4	D6	O	Pixel Array Output bit 6
D5	D9	O	Pixel Array Output bit 9
D6	AGND28	AG	Analog Ground
E1	MGND28	MG	MIPI Ground
E2	OUTCM	O	MIPI clock output -
E3	OUTCP	O	MIPI clock output +
E4	DGND	DG	Digital Ground
E5	RSTB	I	Reset Signal,Low level reset
E6	DVDD15	DP	While "BYPASS" Pin connect to"0",internal power supply 1.5V. While "BYPASS" Pin connect to"1",external power supply 1.5V.
F1	AVDD28	AP	Analog Power 2.8V
F2	MVDD28	MP	MIPI Power 1.8V
F3	MVDD15	MP	External Connect capacitance(1uF)
F4	AGND28	AG	Analog Ground
F5	VSYNC	O	Vertical Sync Signal
F6	AVDD28	AP	Analog Power 2.8V

Table 3 Pin Description

Revision History

Version	Date	Description
Commercial 1.0	2012.12.19	1. The first release for TSV package version
Commercial 1.1	2012.12.21	1. fixed part number mistakes
Commercial 1.2	2013.01.07	1. edit key performance parameters: power consumption
Commercial 1.3	2013.01.14	1. edit pll and clock generator block 2. fixed the frame rate mistake in general description 3. edit frame rate in key performance parameters 4. replaced the function diagram by latest version
Commercial 1.4	2013.01.18	1. edit frame rate in general description and key performance parameter
Commercial 1.5	2013.01.22	1. edit power up/off sequence
Commercial 1.6	2013.01.23	1. edit power up/off sequence