



# AU3841

**USB 2.0 WEB Camera Controller**

**USB 1.1/2.0 compliance**

**VISTA 32/64 DTM compliance**

**Technical Reference Manual**

**Rev. 1.02**

**Oct. 2010**



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**USB 2.0 WEB Camera Controller**

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## Revision History

Date	Revision	Description
Feb. 2010	1.00	Preliminary Release
Oct.2010	1.01	Add 46 Pin QFN package
Oct. 2010	1.02	Update AU3841 46-Pin LQFN Pin out

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**Alcor Micro, Corp.**

**AU3841 USB2.0 Web Camera Controller V1.02**

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**<Memo>**



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# 1. Introduction

## 1.1 Description

The AU3841 is a media product that is a single chip with ultra low cost-effective target for Stand-alone and build-in WEB camera solution. The AU3841 is a USB video compliance chip with OS support UVC standard and USB audio compliance (Window 7, VISTA, XP/SP2). AU3841 also build-in 8KB OTP (One Time Programmable) ROM with partial programmable and 4 CH LDO to achieve totally BOM cost reduction. For Audio solution AU3841 also build-in 1-CH 16 bit ADC and digital MIC input interface

## 1.2 Features

- **USB**

- USB 2.0 & 1.1 compliance
- USB video class V1.1 compliance (UVC)
- USB audio class V1.1 compliance (UAC)
- USB high speed, full speed auto switching.

- **Sensors**

- Support with most popular CMOS sensors
- Support VGA (300K, 640x480), SXGA (1.3M, 1280x1024), UXGA (2M, 1600x1200) and QXGA (3M, 2048x1536)
- Programmable I2C interface for verities sensor

- **Video performance**

### Maximum Frame rate at High Speed with MS UVC Driver

	QXGA	UXGA	SXGA	SVGA	VGA	CIF	QVGA	QCIF	QQVGA
YUY2	4 fps	6 fps	8 fps	24 fps	30 fps	30 fps	30fps	30 fps	30 fps
MJPEG	NA	NA	30 fps	30 fps	60fps	60fps	120 fps	120 fps	120 fps

### Maximum Frame rate at Full Speed with MS UVC Driver

	QXGA	UXGA	SXGA	SVGA	VGA	CIF	QVGA	QCIF	QQVGA
YUY2	NA	NA	NA	NA	NA	5 fps	7 fps	20 fps	26 fps
MJPEG	NA	NA	NA	NA	30 fps	30 fps	30 fps	30 fps	30 fps

- **Audio performance**

		1-CH ADC
High speed	Sample rate	48KHz, 44.1KHz, 24KHz, 22.05KHz, 16KHz, 12KHz, 11.025KHz, 8KHz
	Bit resolution	16-bit
Full speed	Sample rate	8KHz, 16KHz
	Bit resolution	16-bit

- **System**

- **Power**

- ◆ Build-in 5V to 3.3 V Regulator
- ◆ Build-in 3.3 V to 1.8 V Regulator
- ◆ Build-in 3.3 V to 2.8 V on/off control for sensor's power
- ◆ Build-in 3.3 V to 1.8 V on/off control for sensor's power
- ◆ IO power support from 1.8V or 3.3 V



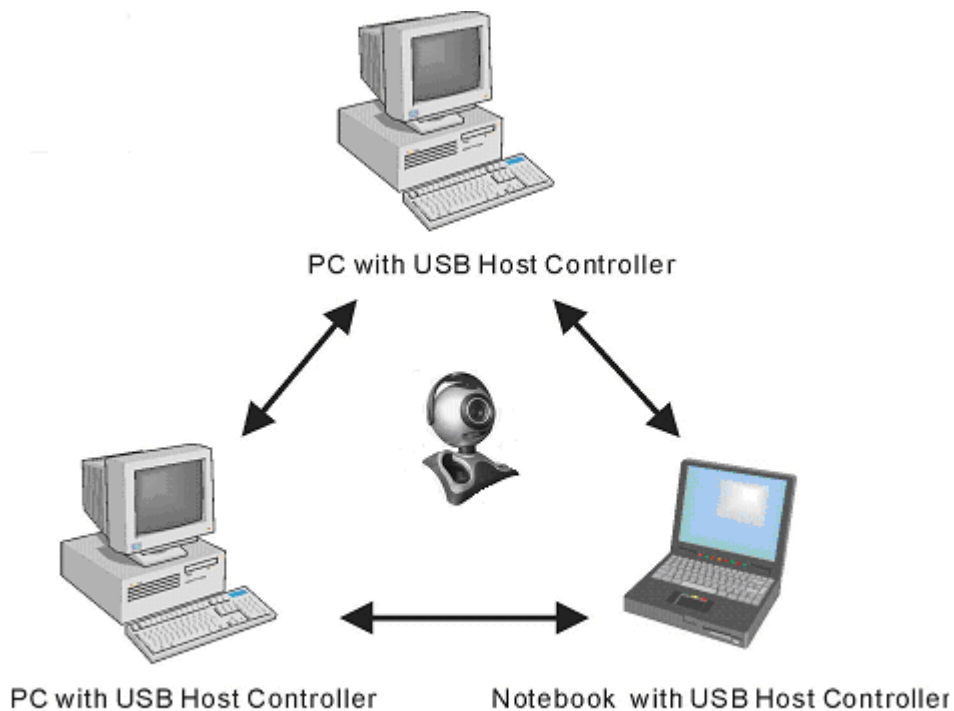
- ◆ Low power consumption
  - Active power < 57 mA (exclude sensor power in S5K6AA 30 fps at VGA)
  - Idle power < 25 mA
  - Suspend power < 350 uA
- Customized VID, PID
- Customized string data
- Support GPIO pins
  - ◆ EEPROM write protect
  - ◆ Sensor reset
  - ◆ Sensor standby
  - ◆ LED indicator
  - ◆ Snapshot
  - ◆ Privacy Mode
- **ISP**
  - **Control**
  - BCHS control
    - ◆ Brightness
    - ◆ Contrast
    - ◆ Hue
    - ◆ Saturation
- **Video Format**
  - **Support sensor format**
    - ◆ YUY2 mode
    - ◆ MJPEG mode
  - **Default UVC driver**
    - ◆ YUY2 mode output
    - ◆ MJPEG mode output
  - **User defined driver**
    - ◆ YUY2 mode output
    - ◆ MJPEG mode output
    - ◆ RGB 24 output
- **External Interface**
  - Support Standard 2/3 wire I2C interface
  - I2C control to EEPROM support from 512 B to 16 KB for sensor setting and firmware upgradeable
  - Support I/F serial flash



- **Software**
  - OS running under Windows 7, Vista, Windows XP SP2 under UVC drive
  - OS running under Windows 7, Vista, Windows XP under UAC drive
  - Support Vendor Driver to support MS Windows 2000 SP4, XP SP1/SP2, VISITA 32/64
  - Support Linux kernel V 2.6.2.1 and later
  - MAC OS 10.4 or later
- **Image Effects ( driver support at YUV output)**
  - Animation Effects
  - Text Effects
  - Face tracking
- **Clock source**
  - 12 M Crystal 3.3 V
- **LOGO Certification**
  - USB high speed logo
  - Windows 7, VISITA, XP DTM logo
- **AP Video filter Control**
  - Brightness
  - Contrast
  - Hue
  - Saturation
  - Gamma
  - Backlight Compensation
  - Anti-Flicker
  - Exposure
  - Low Light Compensation
- **Running under Application software**
  - AMCAP
  - SKYPE
  - MSN
  - QQ massager
  - AIM

## 2. Application Block Diagram

The following figure shows the application diagram of a PC CAMERA product with AU3841. By connecting the USB protocol to a desktop or notebook PC through USB bus, AU3841 is then turned into a bus-powered, full speed, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.



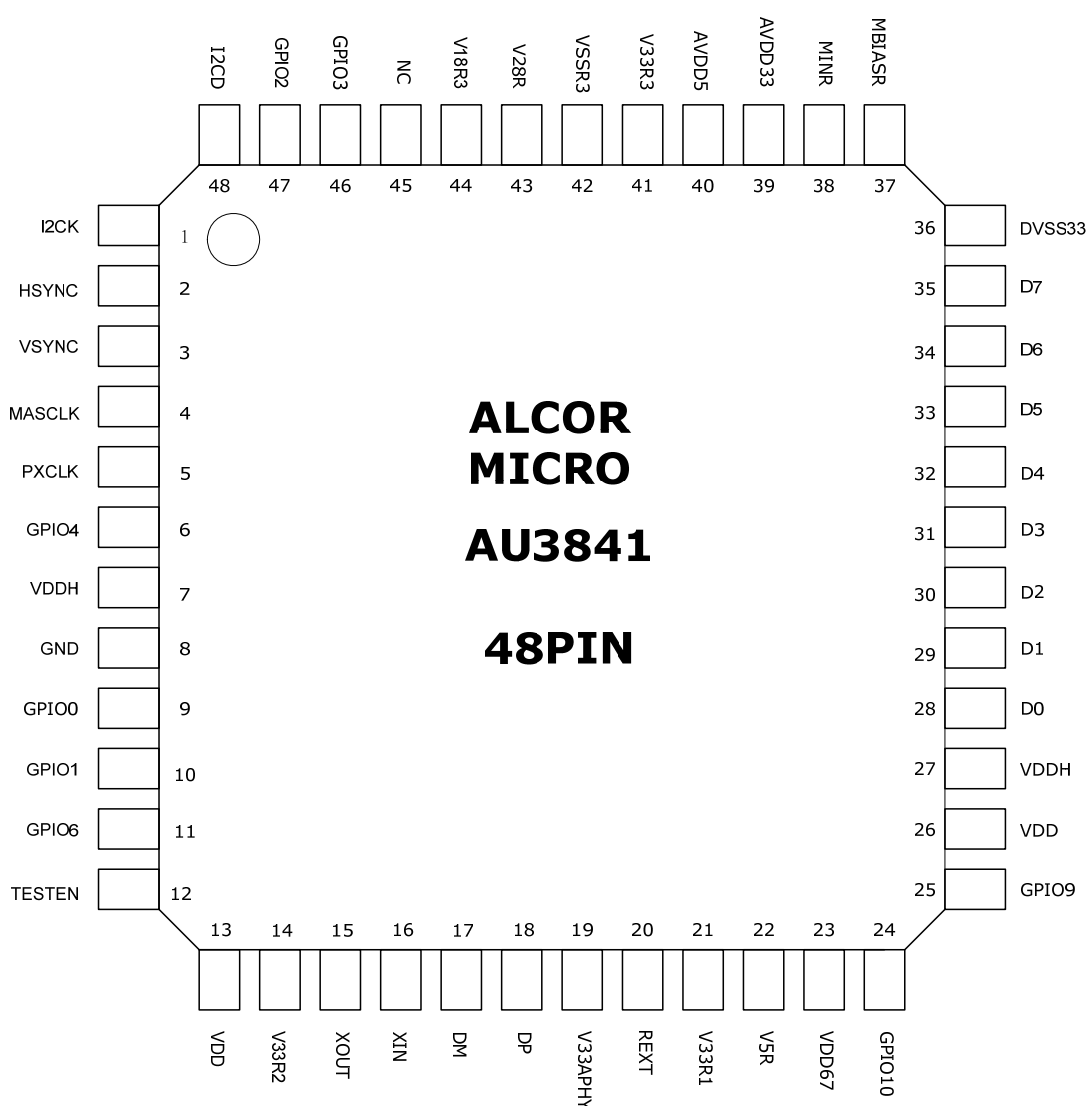
**Figure 2.1 Application Block Diagram**



### 3. Pin Assignment

Depending on the application, the AU3841 is available in two different packages. Below figure shows signal name for each pin and the table in the page after describes each pin in detail.

Figure 3.1 AU3841 48-Pin LQFP Pin Assignment Diagram



**Table 3.1 AU3841 48 Pin Descriptions**

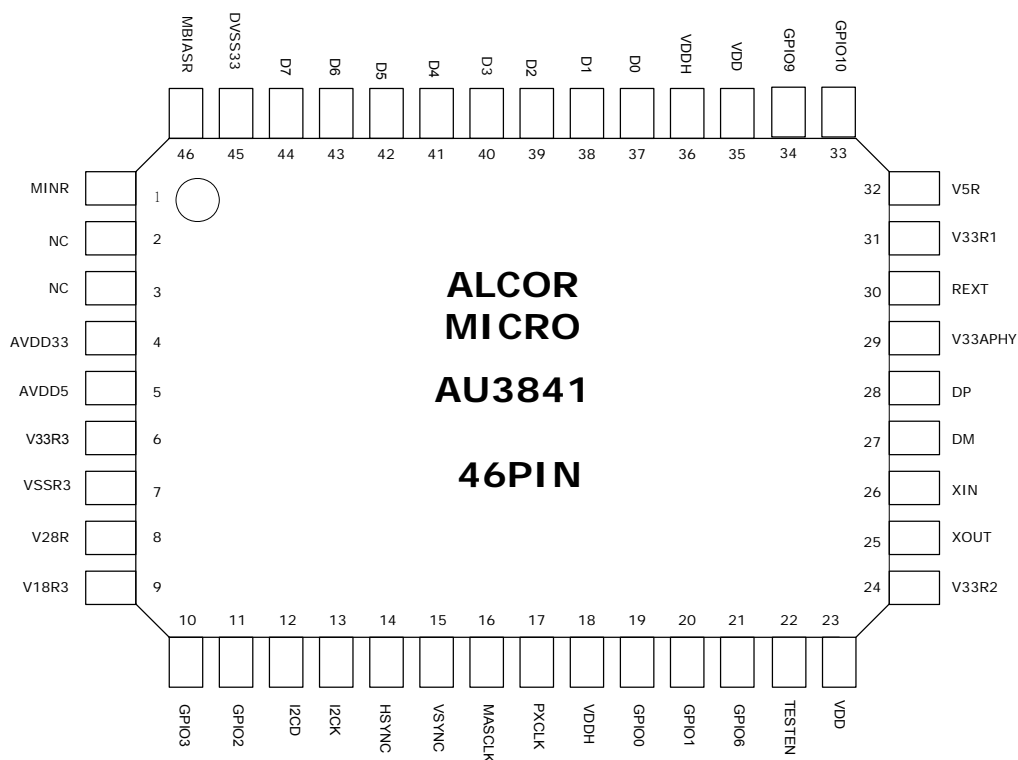
Pin #	Pin Name	I/O	Description
1	I2CK	I/O	I2C interface clock
2	HSYNC	I	HSYNC from sensor
3	VSYNC	I	VSYNC from sensor
4	MASCLK	O	Master clock to sensor
5	PXCLK	I	PXCLK from sensor
6	GPIO4	I/O	General purpose I/O 4
7	VDDH	P	3.3V or 1.8V IO power input
8	GND	P	Digital power ground
9	GPIO0	I/O	General purpose I/O 0
10	GPIO1	I/O	General purpose I/O 1
11	GPIO6	I/O	General purpose I/O 6
12	TESTEN	I	Test mode enable, internal pull down
13	VDD	P	1.8V core power output
14	V33R2	P	3.3V power input
15	XOUT	A	12 MHz crystal output
16	XIN	A	12 MHz crystal input
17	DM	A	USB DM
18	DP	A	USB DP
19	V33APHY	P	3.3V power input
20	REXT	A	External 680 ohm resistor to ground
21	V33R1	P	3.3V power output
22	V5R	P	5V power input
23	VDD67	P	6.7V power input
24	GPIO10	I/O	General purpose I/O 10
25	GPIO9	I/O	General purpose I/O 9
26	VDD	P	1.8V core power input
27	VDDH	P	3.3V or 1.8V IO power input
28	D0	I/O	Sensor data bus 0
29	D1	I/O	Sensor data bus 1



Pin #	Pin Name	I/O	Description
30	D2	I/O	Sensor data bus 2
31	D3	I/O	Sensor data bus 3
32	D4	I/O	Sensor data bus 4
33	D5	I/O	Sensor data bus 5
34	D6	I/O	Sensor data bus 6
35	D7	I/O	Sensor data bus 7
36	DVSS33	P	Analog microphone power ground
37	MBIASR	A	Bias voltage output
38	MINR	A	Analog microphone input
39	AVDD33	P	3.3V power output
40	AVDD5	P	5V power input
41	V33R3	P	3.3V power input
42	VSSR3	GND	Sensor power ground
43	V28R	P	2.8V power output for sensor
44	V18R3	P	1.8V power output for sensor
45	NC	O	
46	GPIO3	I/O	General purpose I/O 3
47	GPIO2	I/O	General purpose I/O 2
48	I2CD	I/O	I2C interface data



Figure 3.2 AU3841 46-Pin LQFN Pin Assignment Diagram



**Table 3.2 AU3841 46 Pin Descriptions**

Pin #	Pin Name	I/O	Description
1	MINR	A	Analog microphone input (right channel)
2	NC		
3	NC		
4	AVDD33	P	3.3V power output
5	AVDD5	P	5V power input
6	V33R3	P	LDO 3.3V power input
7	VSSR3	P	LDO ground
8	V28R	P	LDO 2.8V power output for sensor
9	V18R3	P	LDO 1.8V power output for sensor
10	GPIO3	I/O	General purpose I/O 3
11	GPIO2	I/O	General purpose I/O 2
12	I2CD	I/O	I2C interface data
13	I2CK	I/O	I2C interface clock
14	HSYNC	I	HSYNC from sensor
15	VSNC	I	VSNC from sensor
16	MASCLK	O	Master clock to sensor
17	PXCLK	I	PXCLK from sensor
18	VDDH	P	3.3V or 1.8V IO power input
19	GPIO0	I/O	General purpose I/O 0
20	GPIO1	I/O	General purpose I/O 1
21	GPIO6	I/O	General purpose I/O 6
22	TESTEN	I	Test mode enable, internal pull down
23	VDD	P	LDO 1.8V core power output
24	V33R2	P	LDO 3.3V power input
25	XOUT	A	12 MHz crystal output
26	XIN	A	12 MHz crystal input
27	DM	A	USB DM
28	DP	A	USB DP
29	V33APHY	P	3.3V power input

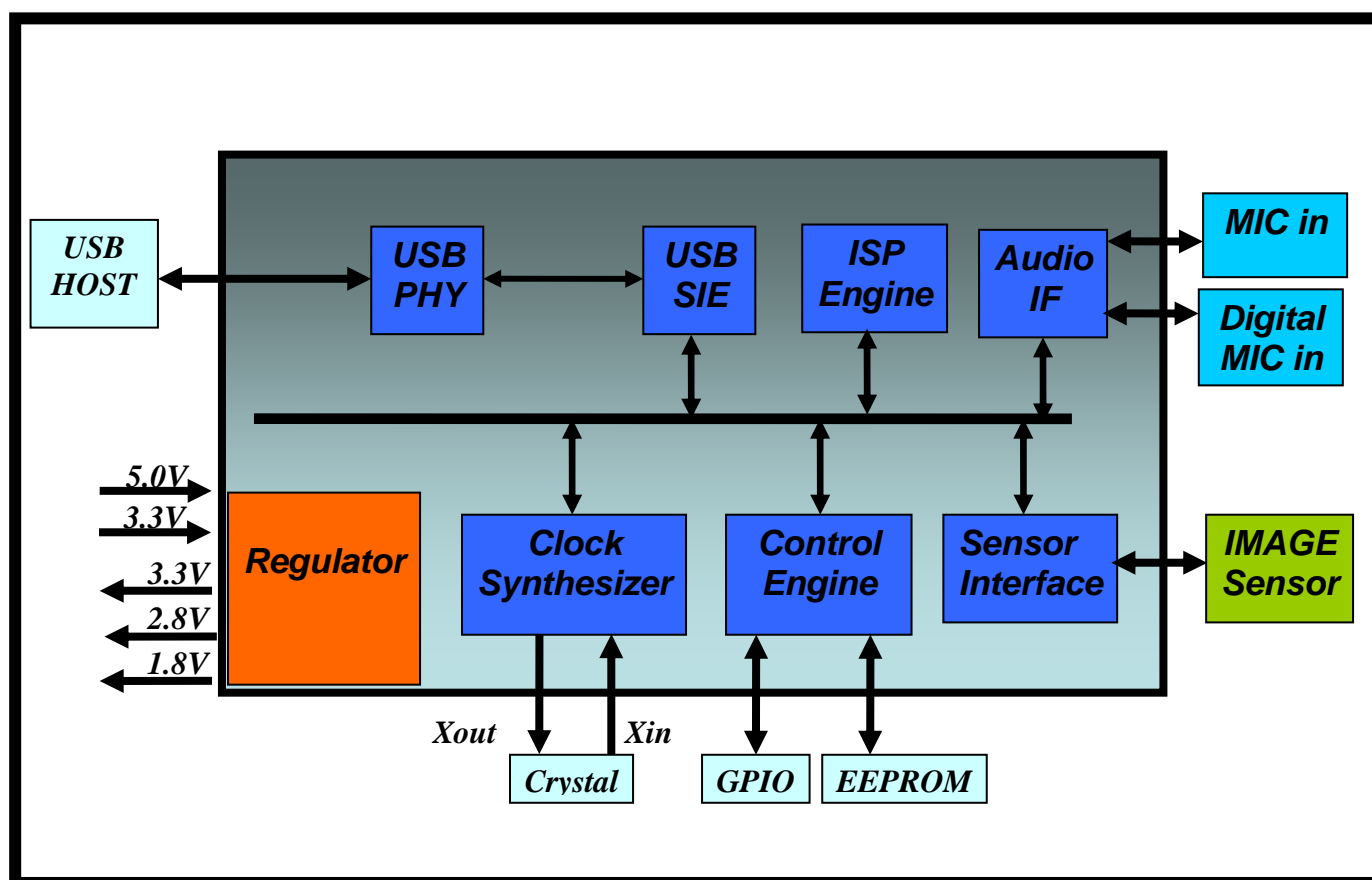


Pin #	Pin Name	I/O	Description
30	REXT	A	External 680 ohm resistor to ground
31	V33R1	P	3.3V regulator output
32	V5R	P	LDO 5V power input , 6.7V power input in internal EPROM programming mode
33	GPIO10	I/O	General purpose I/O 10
34	GPIO9	I/O	General purpose I/O 9
35	VDD	P	1.8V core power input
36	VDDH	P	3.3V or 1.8V IO power input
37	D0	I	Sensor data bus 0
38	D1	I	Sensor data bus 1
39	D2	I	Sensor data bus 2
40	D3	I	Sensor data bus 3
41	D4	I	Sensor data bus 4
42	D5	I	Sensor data bus 5
43	D6	I	Sensor data bus 6
44	D7	I	Sensor data bus 7
45	DVSS33	P	Analog microphone power ground
46	MBIASR	A	Bias voltage output (right channel)

## 4. System Architecture and Reference Design

### 4.1 AU3841 Block Diagram

Figure 4.1 AU3841 Block Diagram





## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DDH}$	Power Supply	-0.3 to $V_{DDH} + 0.3$	V
$V_{IN}$	Input Signal Voltage	-0.3 to 3.6	V
$V_{OUT}$	Output Signal Voltage	-0.3 to $V_{DDH} + 0.3$	V
$T_{STG}$	Storage Temperature	-40 to 150	°C

### 5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V5R	5V Power Supply	4.75	5	5.25	V
$V_{DDH}$	Power Supply	3.0	3.3	3.6	V
		1.62	1.8	1.98	V
$V_{DD}$	Digital Supply	1.62	1.8	1.98	V
$V_{IN}$	Input Signal Voltage	0	3.3	3.6	V
$T_{OPR}$	Operating Temperature	-10		70	°C
$T_{OST}$	Operation surface Temperature	17		85	°C

### 5.3 General DC Characteristics

Table 5.3 General DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{IN}$	Input current	No pull-up or pull-down	-10	$\pm 1$	10	$\mu A$
$I_{OZ}$	Tri-state leakage current		-10	$\pm 1$	10	$\mu A$
$C_{IN}$	Input capacitance	Pad Limit		2.8		$\rho F$
$C_{OUT}$	Output capacitance	Pad Limit		2.8		$\rho F$
$C_{BID}$	Bi-directional buffer capacitance	Pad Limit		2.8		$\rho F$



## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{DDH}$	Power supply	3.3V I/O	3.0	3.3	3.6	V
$V_{il}$	Input low voltage	LVTTTL			0.8	V
$V_{ih}$	Input high voltage		2.0			V
$V_{ol}$	Output low voltage	$ I_{ol}  = 2 \sim 16\text{mA}$			0.4	V
$V_{oh}$	Output high voltage	$ I_{oh}  = 2 \sim 16\text{mA}$	2.4			V
$R_{pu}$	Input pull-up resistance	PU=high, PD=low	55	75	110	$K\Omega$
$R_{pd}$	Input pull-down resistance	PU=low, PD=high	40	75	150	$K\Omega$
$I_{in}$	Input leakage current	$V_{in} = V_{DDH}$ or 0	-10	$\pm 1$	10	$\mu A$
$I_{oz}$	Tri-state output leakage current		-10	$\pm 1$	10	$\mu A$
$I_{3.3vout}$	3.3 V current output	$T = 25^\circ C$			250	mA
$I_{2.8vout}$	2.8 V current output	$T = 25^\circ C$			100	mA
$I_{1.8vout}$	1.8 V current output	$T = 25^\circ C$			100	mA
$I_{3.3vpsrr}$	3.3 V PSRR	$V_{in} / V_{noise}$		40		dB
$I_{2.8vpsrr}$	2.8 V PSRR	$V_{in} / V_{noise}$		40		dB
$I_{1.8vpsrr}$	1.8 V PSRR	$V_{in} / V_{noise}$		40		dB

## 5.5 DC Electrical Characteristics of 1.8V I/O Cells

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{DDH}$	Power supply	1.8V I/O	1.62	1.8	1.98	V
$V_{il}$	Input low voltage	LVTTTL			0.69	V
$V_{ih}$	Input high voltage		1.05			V
$V_{ol}$	Output low voltage	$ I_{ol}  = 2 \sim 16\text{mA}$			0.4	V
$V_{oh}$	Output high voltage	$ I_{oh}  = 2 \sim 16\text{mA}$	1.22			V
$R_{pu}$	Input pull-up resistance	PU=high, PD=low	105	180	330	$K\Omega$



$R_{pd}$	Input pull-down resistance	PU=low, PD=high	105	210	420	$K\Omega$
$I_{in}$	Input leakage current	$V_{in} = V_{DDH}$ or 0	-10	$\pm 1$	10	$\mu A$
$I_{oz}$	Tri-state output leakage current		-10	$\pm 1$	10	$\mu A$

## 5.6 USB Transceiver Characteristics

Table 5.6 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V33APHY	Analog supply Voltage		3.0	3.3	3.6	V
$I_{CC}$	Operating supply current	High speed operating at 480 MHz				mA
$I_{CC} (standby)$	Standby supply current	High speed operating at 480 MHz		20		mA
$I_{CC} (susp)$	Suspend supply current	In suspend mode, current with $1.5k\Omega$ pull-up resistor on pin RPU disconnected			200	$\mu A$

Table 5.7 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
$V_{IL}$	Low-level input voltage			0.8		V
$V_{IH}$	High-level input voltage	2.0			2.0	V
Output levels						
$V_{OL}$	Low-level output voltage				0.2	V
$V_{OH}$	High-level output voltage		VDDH-0.2			V

VD33=3.0V~3.6V ; VDDU,VDDA=1.62V~1.98V ; Temp=0°C~70°C



Table 5.8 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
$V_{HSDIFF}$	High speed differential input sensitivity	$ V_{I(DP)}-V_{I(DM)} $ measured at the connection as application circuit	300			mV
$V_{HSCM}$	High speed data signaling common mode voltage range		-50		500	mV
$V_{HSSQ}$	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
$V_{HSDSC}$	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
$V_{HSOI}$	High speed idle level output voltage(differential)		-10		10	mV
$V_{HSOL}$	High speed low level output voltage(differential)		-10		10	mV
$V_{HSOH}$	High speed high level output voltage(differential)		360		440	mV
$V_{CHIRPJ}$	Chirp-J output voltage (differential)		700		1100	mV
$V_{CHIRPK}$	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
$R_{DRV}$	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	$\Omega$
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
$V_{TERM}$	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
$V_{DI}$	Differential input sensitivity	$ V_{I(DP)}-V_{I(DM)} $	0.2			V
$V_{CM}$	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						
$V_{SE}$	Single ended receiver threshold		0.8		2.0	V
Output levels						
$V_{OL}$	Low-level output voltage		0		0.3	V



Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	High-level output voltage		2.8		3.6	V

VDD33=3.0V~3.6V ; VDDU,VDDA=1.62V~1.98V ; Temp=0°C~70°C

Table 5.9 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
$t_{HSR}$	High-speed differential rise time		500			ps
$t_{HSF}$	High-speed differential fall time		500			ps
Full-Speed Mode						
$t_{FR}$	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FF}$	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FRMA}$	Differential rise/fall time matching ( $t_{FR} / t_{FF}$ )	Excluding the first transition from idle mode	90		110	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
$t_{LR}$	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $ ;	75		300	ns
$t_{LF}$	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $ ;	75		300	ns
$t_{LRMA}$	Differential rise/fall time matching ( $t_{LR} / t_{LF}$ )	Excluding the first transition from idle mode	80		125	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
$V_{OH}$	High-level output voltage		2.8		3.6	V

## 6. Mechanical Information

Figure 6.1 48 Pin LQFP Mechanical Information Diagram

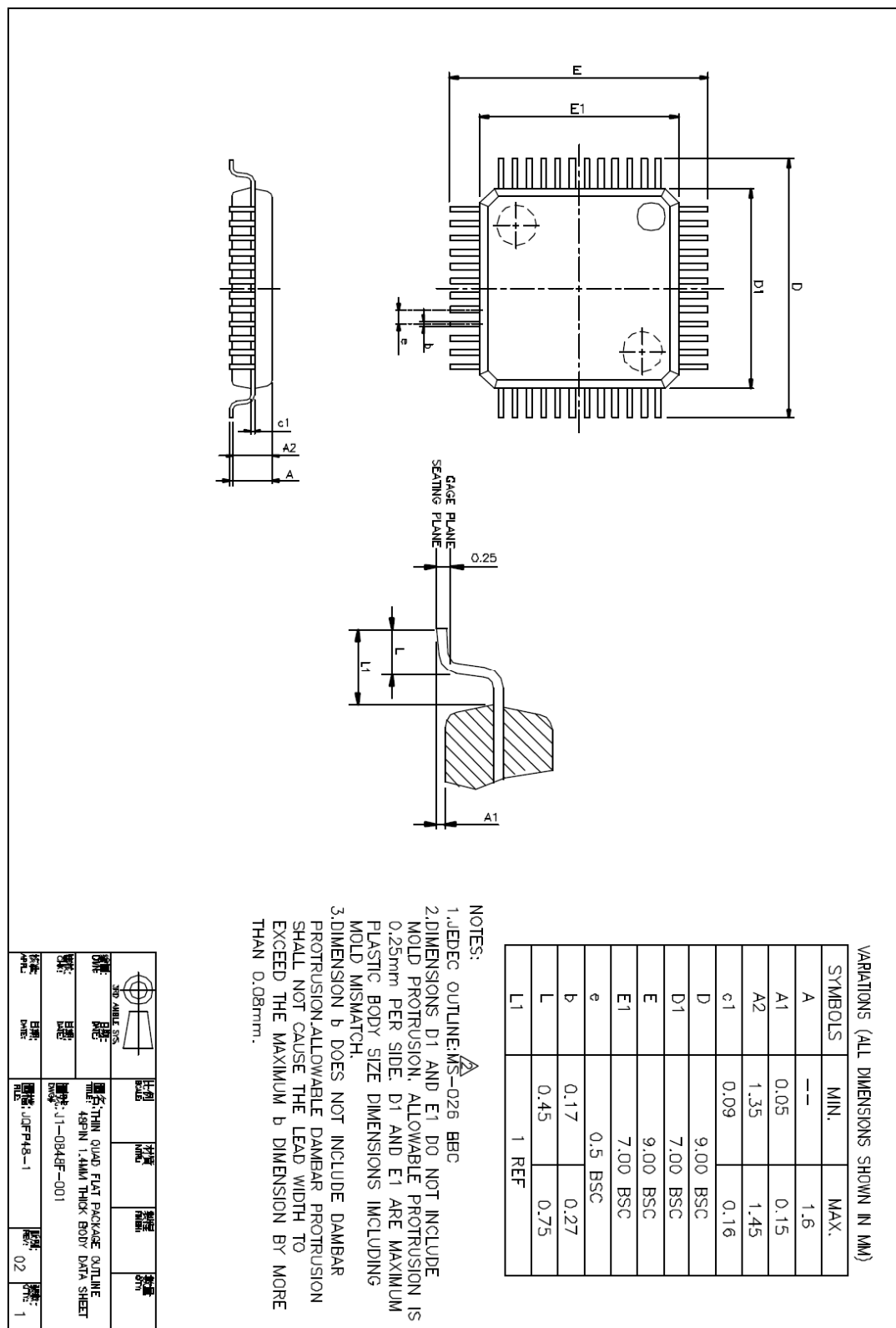
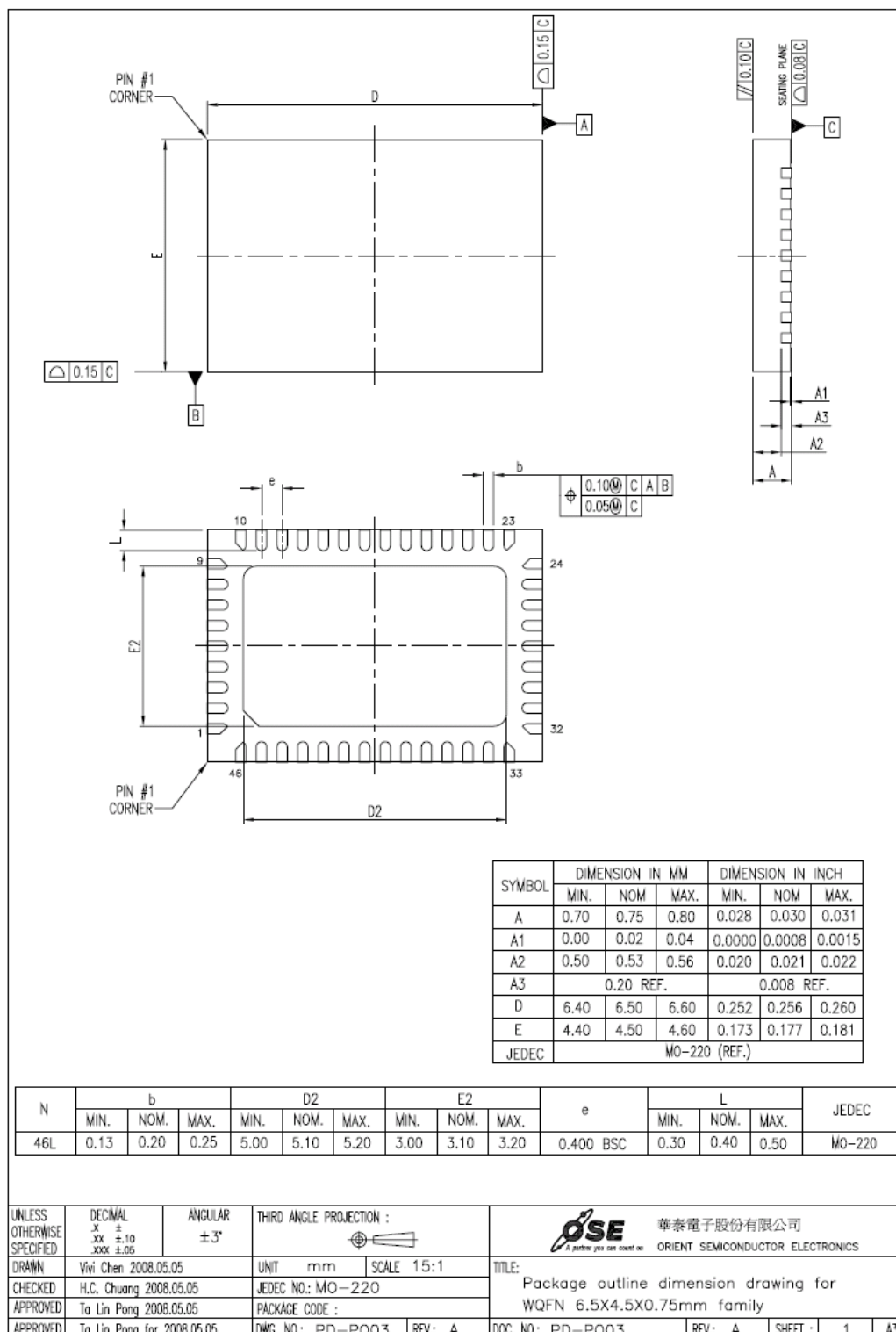


Figure 6.3 46 Pin LQFN Mechanical Information Diagram





## 7. Ordering Information

Ordering Part Number	Package	Lead material	Package method
AU3841-GBL-GR	LQFP48	Green	Tray
AU3841-GAN-GR	LQFN46	Green	Tray

## 8. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

<b>DC Electrical</b>	Direct Current Electrical
<b>PLL</b>	Phase Lock Loop, which is a closed-loop frequency control system
<b>XTAL</b>	Crystal
<b>UVC</b>	USB Video Class

## About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.