



1/7-Inch 0.3 Mega Pixel Image Sensor SP0718

Specification

Version Commercial 1.0

2012.11.16

SuperPix Micro Technology Co., Ltd

SuperPix 1/7 – Inch 0.3Mega Pixel Image Sensor

1/7-Inch 0.3 Mega Pixel Image Sensor

Part Number SP0718

SuperPix® SP0718 is a 1/7 inch, 0.3 mega pixel color image sensor chip with a brand new pixel structure and an improved image signal processor (ISP). SP0718 produces extraordinarily refined digital pictures, and its ability to capture both video and single images makes it the perfect choice for a wide range of mainstream consumer applications, especially for tablet computers or notebook computers market. SP0718 is base on the SuperPix® latest sensor pixel architecture design (3.2um x 3.2um size) that can cope with problems generated by rough environment light conditions and deliver excellent pictures. The markedly appropriately chip size of SP0718 will make it become a critical role of VGA format in portable equipment realm. As far as the digital image signal processor is concerned, SP0718 also launches a new era by improving most of its pre processing functionalities.

Functionalities

- CMOS Image Sensor
- Image Signal Processor

Applications

- Tablet Cam
- Notebook Cam
- PC Cam
- Web Cam
- Toys



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Overview

General Description

SuperPix® SP0718 is a 1/7 inch, 0.3 mega pixel color image sensor chip with a brand new pixel structure and an improved image signal processor (ISP). SP0718 produces extraordinarily refined digital pictures, and its ability to capture both video and single images makes it the perfect choice for a wide range of mainstream consumer applications, especially for tablet computers or notebook computers market. SP0718 is base on the SuperPix® latest sensor pixel architecture design (3.2um x 3.2um size) that can cope with problems generated by rough environment light conditions and deliver excellent pictures. The markedly appropriately chip size of SP0718 will make it become a critical role of VGA format in portable equipment realm. As far as the digital image signal processor is concerned, SP0718 also launches a new era by improving most of its pre processing functionalities.

SuperPix® is always trying to enhance the domestic image sensor productions and technology. A high performance system on a chip (SOC) sensor, SP0718 is designed specifically to meet the demands of the rapidly growing features of entry-level and mainstream handset market. SP0718 image signal processor includes advanced auto white balance, refined image sharpen and smoothing function, bad pixel cancellation based on improved algorithm, upgraded auto exposure control that supports an exposure time less than that of one row, which can avoid the overexposure phenomenon, and so forth. Additionally, it also features all standard image quality controls such as color saturation, hue, gamma, and noise cancellation. Further more, SP0718 capable of delivering images at 30 frame per second in 640 x 480 (VGA mode) through a high speed parallel interface, which can contribute the high image quality for users. And a serial interface is embedded in as well for accepting the output QVGA data from other sensor, which is a notable feature for dual sensor model.

An overview of the SP0718 Image Sensor features and functions will be given below.

Function Diagram

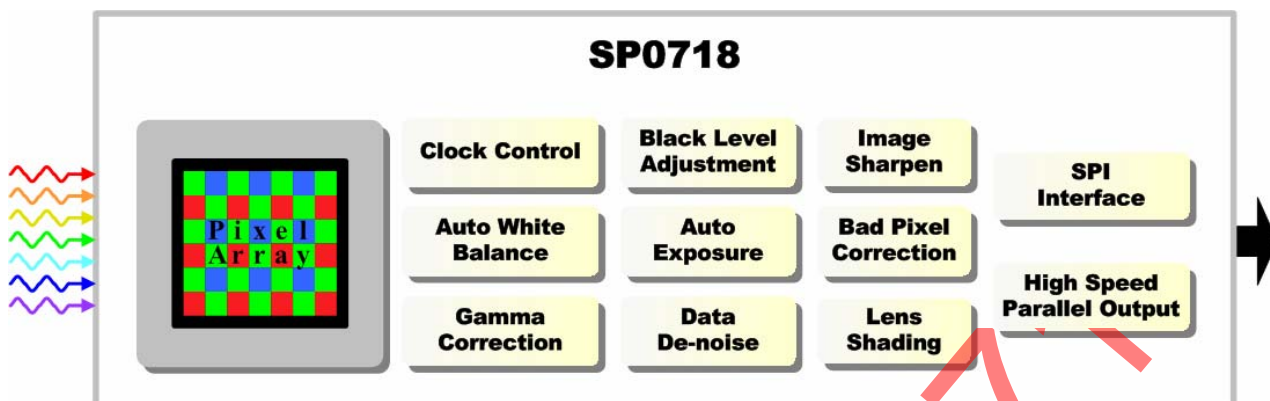


Figure 1 Function Diagram

Typical Application List

- Camera
- Camcorder
- PC Camera
- Mobile Phone
- Toys

Typical Application Diagram



Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	640 x 480
Pixel Size	3.2um x 3.2um Square Pixel
Lens Size	1/7 inch
Color Filter	Primary Color Filter Bayer arrangement
Power Supply	I/O 1.7V ~ 3.0V
	Analog 2.6V ~ 3.0V
Power Consumption	Active TBD
	Standby TBD
Data Formats	CCIR656/601
	YUV422
	RGB565
	RAW8
Output Format	8bit Parallel
Input Clock	6 -27 MHz
Max. Frame Rate	30fps@VGA Mode
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	TSV / COB

Table 1 Key Performance Parameters

Features List

- Active pixel array 640 x 480
- Prominent 3.2um x 3.2um pixel structure
- Analog gain range is 1.0x – 15.5x
- Support 1/4 and 1/16 sub sample function
- Embedded crosstalk compensation arithmetic
- Embedded image preprocessor functionality
 - Automatic Black Level Calibration
 - Automatic White Balance
 - Automatic Exposure Control
 - Automatic Black Level Correction
 - Gamma Correction
 - Lens Shading Compensation
 - De-mosaic Function
 - De-noise Function
 - Color Correction Function
 - Bad Pixel Correction
- I²C bus controlling registers inside chip
- Support QVGA image data input
- Parallel data output

Function Description

Pixel Array Structure

The SP0718 pixel array is configured as of 660 columns by 514 rows, shown below. There are 640 columns by 480 rows of optically active pixels.

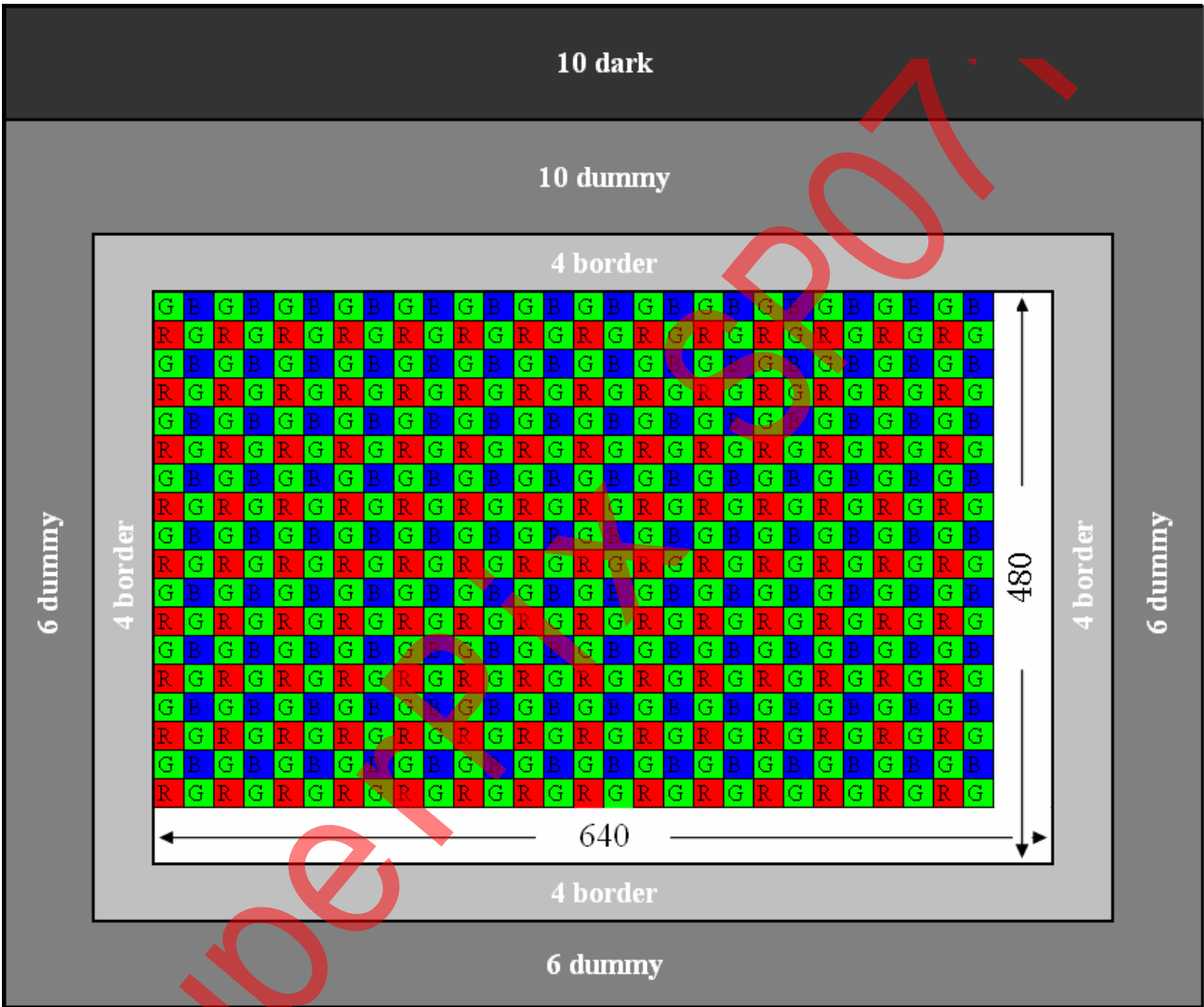


Figure 3 Pixel Floor Plan

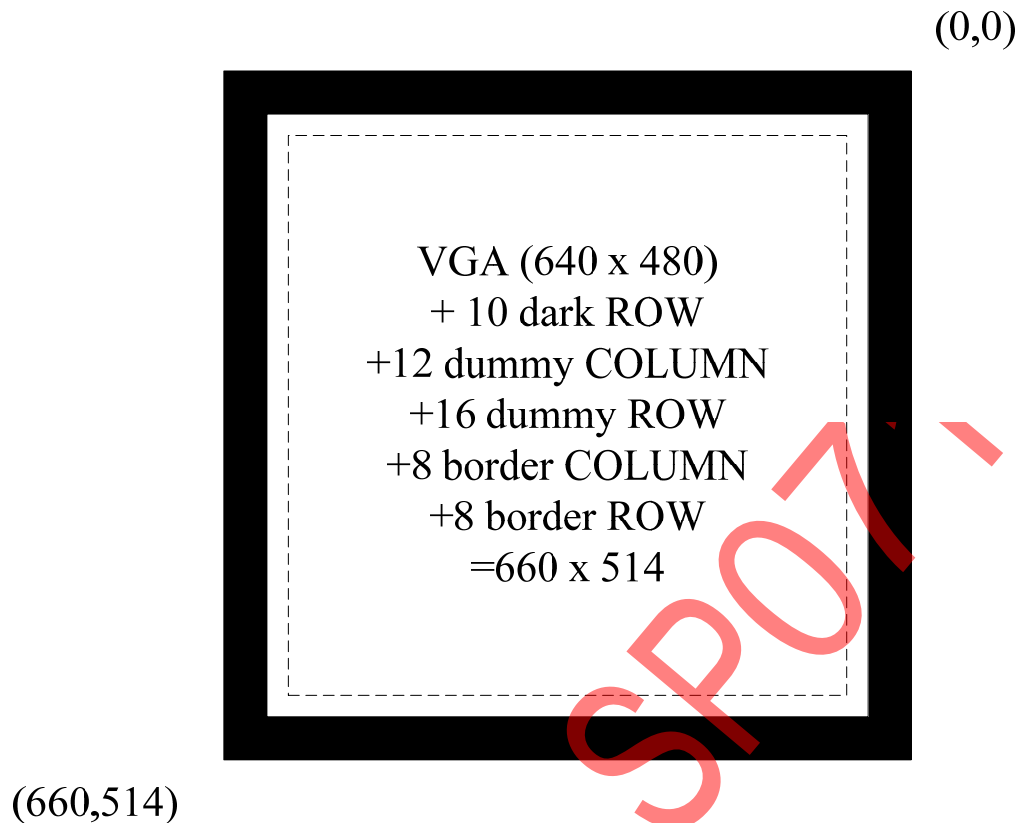


Figure 4 Sensor Pixel Description

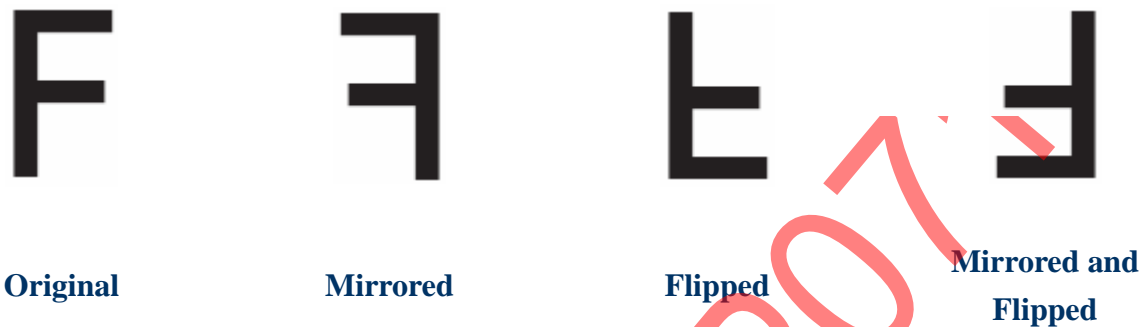
Image Signal Processing Function

- Mirror and Flip
- Windowing
- Test Pattern
- Automatic Black Level Calibration
- Automatic White Balance
- Automatic Exposure Control
- Automatic Black Level Correction
- Gamma Correction
- Lens Shading Compensation
- De-mosaic Function
- De-noise Function
- Color Correction Function
- Bad Pixel Correction
- RGB to YUV Conversion
- YUV to RGB Conversion
- Special Effect

- Parallel Interface

Mirror and Flip

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.



Windowing

The embedded windowing function extract an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By property setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Automatic Black Level Calibration

The pixel array contains several optically black lines, which can be seen at the pixel array structure section. These lines are used to provide the data for black level calibration and further correction.

Automatic White Balance

Auto white balance unit is help to remove the unrealistic color from the image automatically by referencing the white balance pre-gain. With auto white balance unit, the still / video camera system can determine the color temperature of the light and automatically adjust for the color temperature.

Automatic Exposure Control

After Gamma unit, the Y value, calculated by R, G, and B values, used to evaluate the luminance and exposure time, digital gain, analog gain are adjusted by this block to get the right luminance for the image.

Automatic Black Level Correction

Black level correction unit provide the function which is to adjust the black level of the image from the sensor automatically or manually. In this unit, the blackest level will be detected first, than will be used to compare with all pixels.

Gamma Correction

The main purposed of the Gamma correction function is to compensate the characteristics of the sensor. According to de gamma curve, the pixel values can be converted in order to compensate the sensor output on different light strength conditions.

Lens Shading Compensation

Lens imperfection can be eliminated by lens shading compensation. It starts with the first pixel of a frame when the lens shading compensation unit is enabled, and correcting each pixel with its gain values.

The lens shading correction is based on one or more reference frames which have to be captured under dedicated light conditions and a dedicated position of the sensor. The pixels of the captured frame are then evaluated by software and the calculated parameters for lens shading correction are stored in different tables. It is also possible to use different lens shading correction parameters for different environment conditions. Therefore additional reference frames for the different conditions are to be captured and evaluated. The calculated parameters including sector settings can be stored in multiple tables.

De-mosaic Function

De-mosaic function is to convert the raw data to RGB image data. The algorithm is a digital image process used to interpolate a complete image from the partial raw data received form the color filter in form of a matrix of colored pixels. Each raw pixel

data is converted to RGB value using an edge-sensitive color interpolation algorithm.

De-noise Function

The de-noise function can reduce the noise existing on edges markedly and smooth the shades.

Color Correction Function

The color correction function is including various color profiles that are used for color representation improvement. The function works by making decision based on scene brightness and illumination type.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit. A bad pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

RGB to YUV Conversion

It is used to convert the RGB color space to YUV color space so that the following image processing can be done in the YUV color space.

YUV to RGB Conversion

This block converts YUV to RGB so that the ISP can output RGB directly.

Special Effect

A set of image special effect is supported which includes monochrome, negative, sepia and emboss.

Parallel Interface

Parallel Interface defines an interface between a peripheral device and a host processor. The parallel interface tends to be the output interface of most camera devices, and can be configured to operate as a camera interface. This sensor is built

on the heritage and experience in the concept of high quality Superpix[®] traditional high speed parallel interface.

I²C Bus

Single READ and Single WRITE

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

The write-mode address of SP0718 is 42H, and the read-mode address of that is 43H.

Two figures that is shown below will illustrate SP0718 single READ sequence and single WRITE sequence.

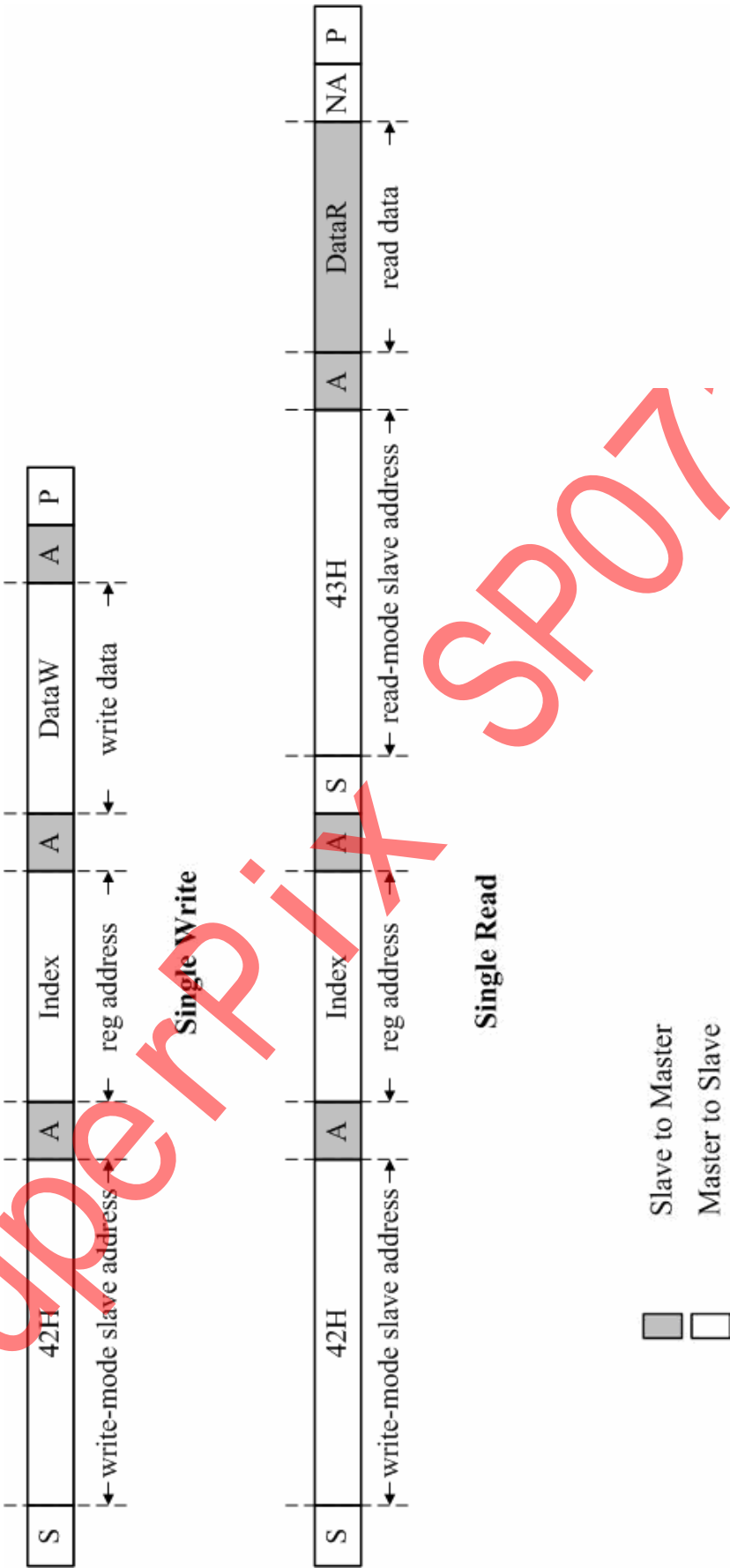


Figure 5 I²C Read & Write Description

Start/Stop Conditions

The serial bus will recognize logic 1 to logic 0 transition on the SDA pin while the SCLK pin is at logic 1 as the start condition. A logic 0 to logic 1 transition on the SDA pin while the SCLK pin is at logic 1 is interrupted as the stop condition.

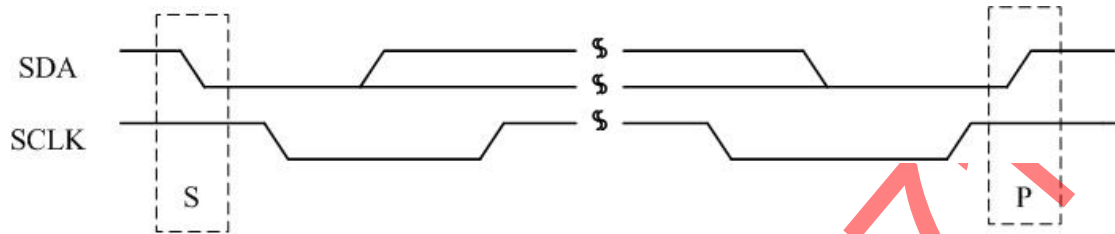


Figure 6 I²C Start & Stop Description

Acknowledge Bit

The SP0718 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

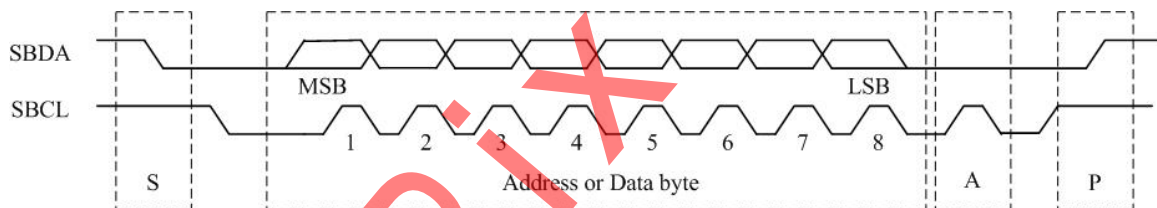


Figure 7 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is "0".

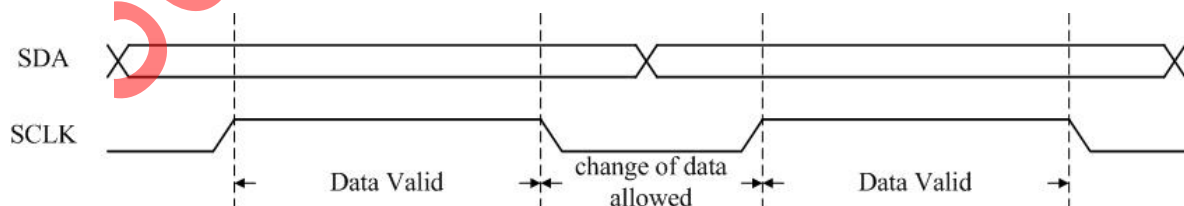


Figure 8 I²C Data Transport Description

Timing Parameter

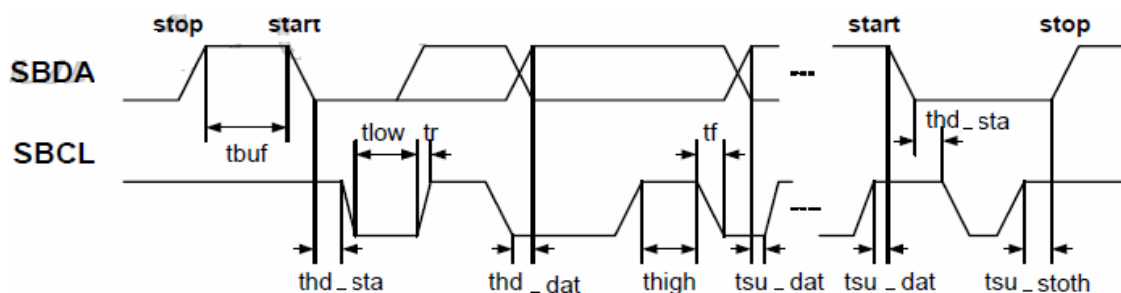


Figure 9 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

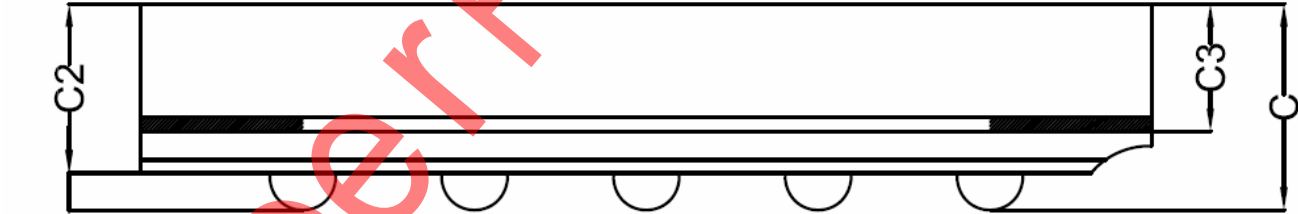
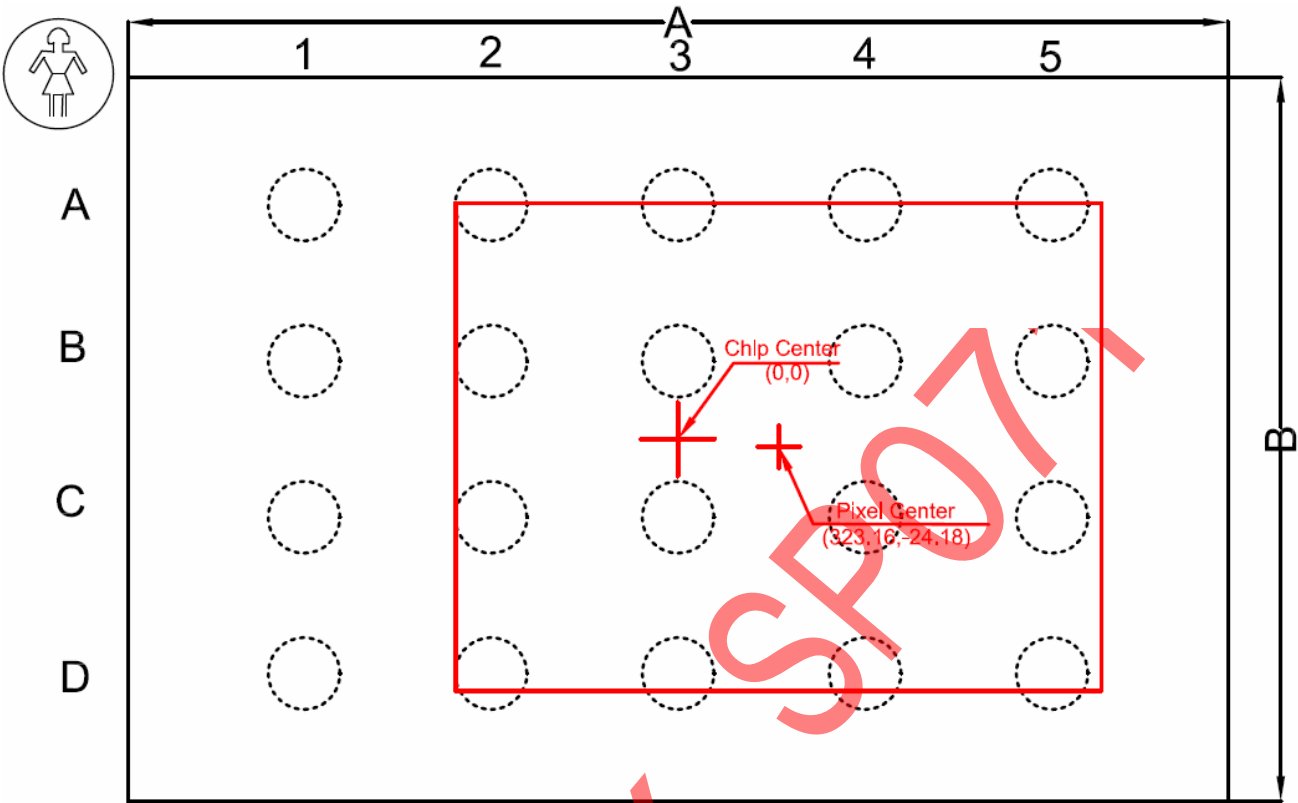
DC Specifications

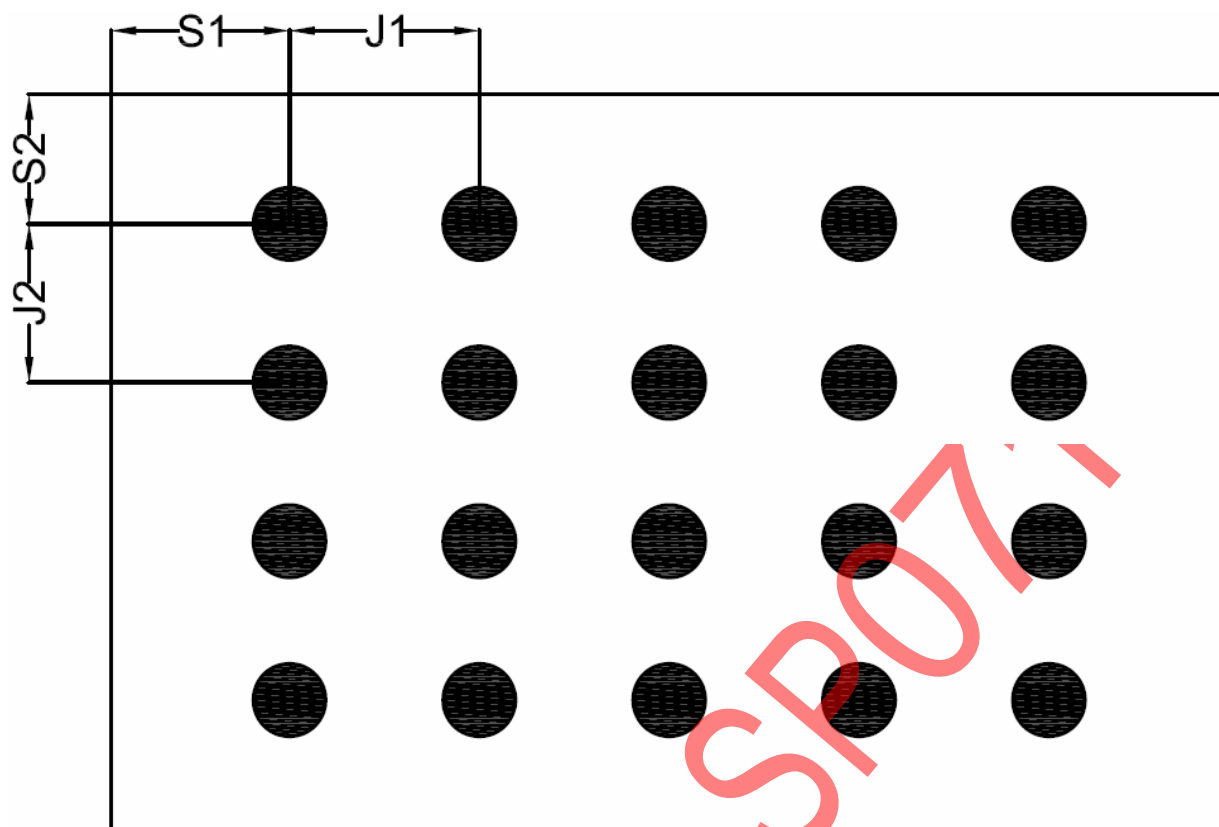
Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.7	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		0.3xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			0.3xVDDIO	V
T	Junction Temperature	-20	25	70	°C

Examination Item

No.	Reliability Items	Condition
1	Temp Cycle	-20°C ~ 70°C each 30 min, 24 cycles
2	High Temp. & Humidity storage	70°C / 80% / 72Hr
3	Low Temp. & Humidity storage	-20°C / 96Hr natural dry, for 3 hours
4	High Temp Operating	70°C / 80% / 72Hr / 2.8V other pins are active condition
5	Low Temp Operating	-20°C / 72Hr / 2.8V other pins are active condition
6	Drop Test	1.5m drop, 1 X 6 plane (Camera with 100g cradle)
7	Random Vibration	5~100HZ, 3 axis (X,Y,Z),15min/axis,swing :6mm

Package





Bottom View
(bumps up)

Figure 10 Package

Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	3529	3504	3554
Package Body Dimension Y	B	2317	2292	2342
Package Height	C	720	660	780
Ball Height	C1	130	100	160
Package Body Thickness	C2	590	555	625
Thickness of glass surface to wafer	C3	445	425	465
Ball Diameter	D	230	200	260
Total Ball count	N	20	—	—
Pin pitch X axis	J1	600	—	—
Pin pitch Y axis	J2	500	—	—
Edge to Pin Center Distance along X	S1	564.5	535	595
Edge to Pin Center Distance along Y	S2	408.5	379	439

Table 2 Package Dimension

	1	2	3	4	5
A	D1	D3	DGND	ECLK	PWDN
B	D0	PLCK	DVDD28	HSYNC	SBDA
C	D2	D4	D6	D7	AVDD
D	SPI_CLK	D5	VSYNC	SBCL	AGND

Table 3 Ball Matrix

PAD	Pin Name	I/O	Pin Description
A1	D1	O	Pixel Array Output Bit 1
A2	D3	O	Pixel Array Output Bit 3
A3	DGND	DG	Digital Ground
A4	ECLK	I	Input system Clock
A5	PD	I	Power down, 0" normal "
B1	D0	O	Pixel Array Output Bit 0
B2	PCLK	O	Pixel Output Clock
B3	DVDD28	DP	Digital I/O Power 2.8V
B4	HSYNC	O	Horizontal Sync Signal
B5	SBDA	I/O	Slave Tri-state, I2C Data Bus
C1	D2	O	Pixel Array Output Bit 2
C2	D4	O	Pixel Array Output Bit 4
C3	D6	O	Pixel Array Output Bit 6
C4	D7	O	Pixel Array Output Bit 7
C5	AVDD	AP	Analog Power 2.8V
D1	SPI_CLK	I	SPI clock
D2	D5	O	Pixel Array Output Bit 5
D3	VSYNC	O	Vertical Sync Signal
D4	SBCL	I	Slave I ² C clock Bus
D5	AGND	AG	Analog Ground

Table 4 Pin Description

Revision History

Version	Date	Description
Commercial 1.0	2012.11.16	1. The first release for customers

Superpix SP0718