1/4 Inch 5 Mega CMOS Image Sensor
SP5408

Specification

Version Commercial 1.1

2013.07.05

SuperPix Micro Technology Co., Ltd

1/4 Inch 5 Mega CMOS Image Sensor Part Number SP5408

The SP5408 is SuperPix®'s latest launched CMOS color image sensor product. It is a high performance 1/4 inch 5-megapixel image sensor based on an advanced 1.4um pixel architecture. The SP5408 is a high cost-performance image sensor product that can be embedded in portable equipment, especially suitable for high-end and mainstream smart phones and tablet computer applications. The SP5408 consists of 2592 x 1944 effective pixels, advanced low power analog circuits (ASP), and a 2-lane MIPI interface - Mobile Industry Processor Interface. The on chip ISP circuits performs sophisticated signal processing including improved black level calibration, lens shading function, bad pixel correction, 2x2 binning function, etc. SP5408 supports high frame speed up to 15fps at full resolution (2592 x 1944) and 30fps at 1080P format (1920 x 1080) transferred over a 2-lane MIPI Interface or a traditional high speed parallel interface.

Functionalities

- CMOS Image Sensor

Applications

- Mobile Phone Camera
- Tablet Camera
- Notebook Camera
- Digital Camera
- Video Camcorder
- PC Camera
- Web Camera

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Overview

General Description

SuperPix® SP5408 is a low-cost, high performance 1/4 inch 5 Mega pixels image sensor, which is the latest production derived from SuperPix® the 2nd generation CMOS image sensor technology. It is loaded with sophisticated features such as advanced 1.4um pixel structure which is a significant breakthrough on the cutting edge of domestic pixel technology, and improved image signal processor delivering excellent image performance and plenty of new functions. The SP5408 is based on the 1.4um x 1.4um CMOS image sensor pixel architecture by proprietary design of SuperPix®, making it an ideal choice for high-end and mainstream smart phone. Further more, the embedded two lanes MIPI interface enables rapid data transfer, increasing reliability, reducing power consumption and also eliminating facility compatibility issues.

In order to Extend SuperPix®'s strategy of high quality and high-end sensor for smart phone market and relative portable equipments , several efficient features enables the SP5408 to achieve best-in-class 5 Mega images and videos. The advanced 1.4um pixel architecture delivers a number of performance improvements over the proprietary technology, in terms of increased sensitivity per unit area, improved quantum efficiency, and reduced crosstalk. Based on those considerable merits, with perfect low-light performance, SP5408 enables a new generation of high-performance camera phone that deliver top quality digital photographs.

All though SP5408 is a RAW sensor, it includes a variety of image control functions, for instance, upgraded black level calibration, refined lens shading function, bad pixel correction, 2 x 2 binning function, and so forth, all of which lead to significant improvement in image quality, even in the most challenging lighting conditions. Moreover, SP5408 supports high frame speed up to 15fps at 2592 x 1944 (5 Mega, QSXGA) resolution and 30fps at 1920 x 1080 (2 Mega, 1080P) resolution transferred over a 2-lane MIPI interface - Mobile Industry Processor Interface, which can deliver the high image quality to users swiftly. These prominent features integrated in SP5408 will result in vivid still and video

images, and make it an effective solution for ultra-slim camera designs for next-generation mobile handsets, smart phones and tablets.

An overview of the SP5408 Image Sensor features and functions will be given below.

Function Diagram

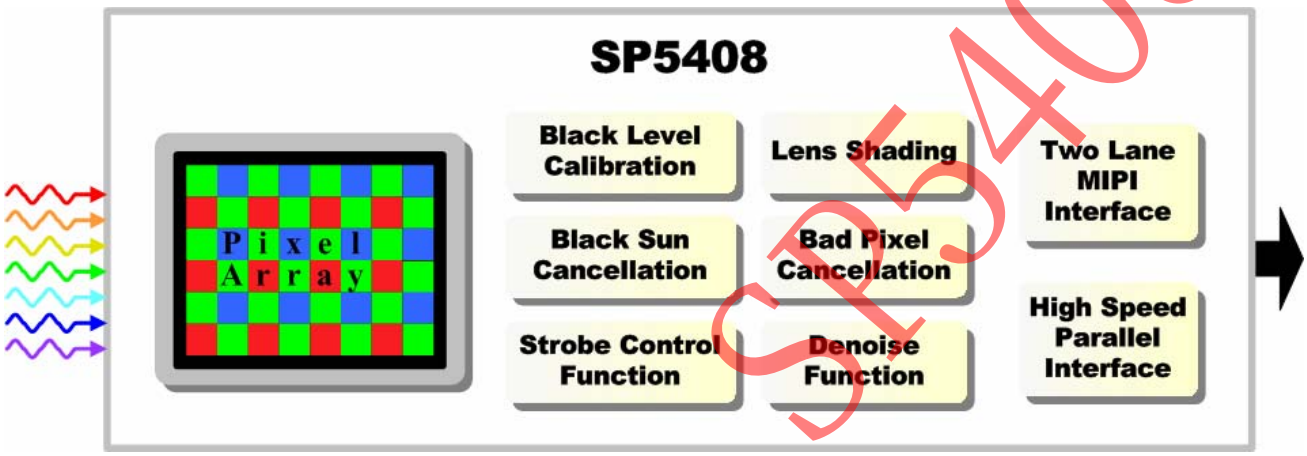


Figure 1 Function Diagram

Typical Application List

- Mobile Phone Camera
- Tablet Camera
- Notebook Camera
- Digital Camera
- Video Camcorder
- PC Camera
- Web Camera
- Toys

Typical Application Diagram

Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	2592 x 1944
Pixel Size	1.4um x 1.4um Square Pixel
Lens Size	1/4 inch
Color Filter	Primary Color Filter Bayer arrangement
Power Supply	I/O 1.7V ~ 3.0V
	DVDD18 1.7V ~ 3.0V
	Analog 2.6V ~ 3.0V
Power consumption	Active TBD
	Standby TBD
Data format	Raw8
	Raw10
Output Formats	CSI-2 2lanes
Input Clock	10 – 30 MHz
Max. Frame Rate	15fps@2592 x 1944 Mode
	30fps@1920 x 1080 Mode
	30fps@1296 x 972 Mode
	30fps@1280 x 720 Mode
Shutter	Rolling Shutter
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	COB / TSV

Table 1 Key Performance Parameters

Features List

- Active pixel array 2592 x 1944
- Advanced 1.4um x 1.4um pixel architecture
- Support night mode
- Support embedded black level calibration
- Support lens shading function
- Support bad pixel cancellation
- Support black sun cancellation
- Support mirror and flip function
- Support strobe control function
- Support horizontal and vertical sub-sample
- Support 8bit and 10bit raw image data output
- Support I²C bus controlling registers inside chip
- Support 2x2 binning function
- Support 2-lane MIPI interface
- Support mainstream mobile phone platforms

Function Description

Pixel Array Structure

The SP5408 pixel array is configured as of 2628 columns by 2026 rows, and the effective array size is 2592 x 1944, while the active array size is 2608 x 1960. The details of pixel array are shown below.

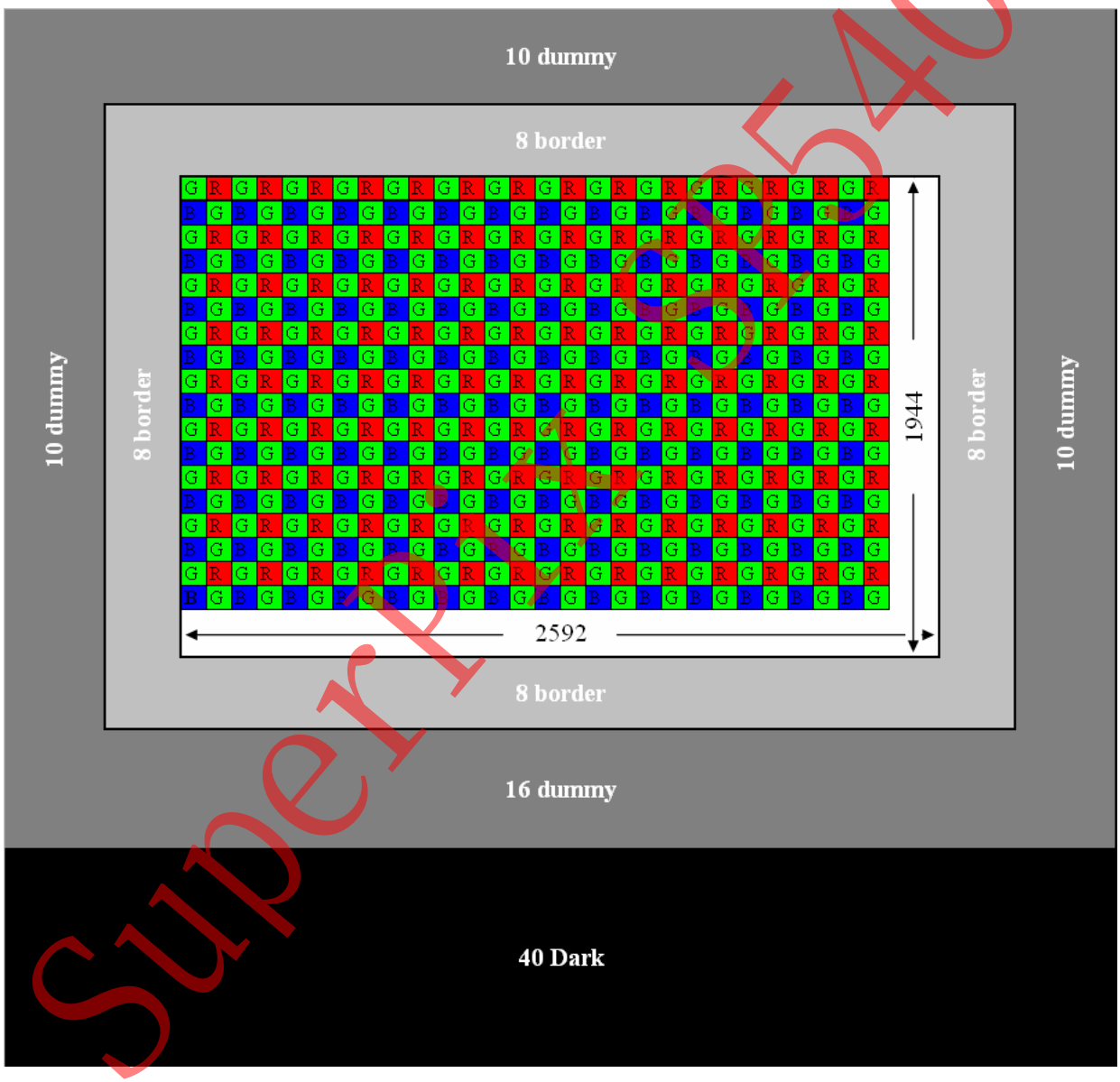


Figure 3 Pixel Floor Plan

Note:
The color filter of the first pixel at left bottom is blue.

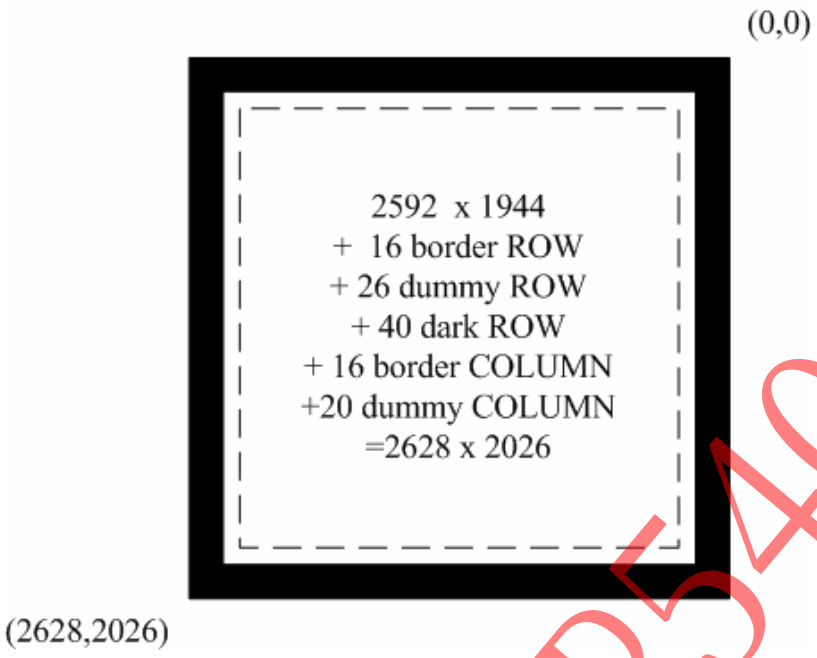


Figure 4 Sensor Pixel Description

Sensor Image Signal Processor Functionality

- Mirror and Flip
- Windowing
- Test Pattern
- Automatic Black Level Calibration
- Lens Shading Compensation
- Denoise Function
- Bad Pixel Correction
- Strobe Control

Mirror and Flip

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.

Original Mirrored Flipped Mirrored and Flipped

Windowing

The embedded windowing function extract an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By property setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Auto Black Level Calibration

The pixel array contains several optically black lines, which can be seen at the pixel array structure section. These lines are used to provide the data for black level calibration and further correction.
When the strobe signal is triggered in mode 2, the strobe signal will be launched immediately, and the next frame – the one is colored shown at the figure above – then can be exposed accurately.

Lens Shading Compensation

Lens imperfection can be eliminated by lens shading compensation. It starts with the first pixel of a frame when the lens shading compensation unit is enabled, and correcting each pixel with its gain values.

The lens shading correction is based on one or more reference frames which have to be captured under dedicated light conditions and a dedicated position of the sensor. The pixels of the captured frame are then evaluated by software and the calculated parameters for lens shading correction are stored in different tables. It is also possible to use different lens shading correction parameters for different environment conditions. Therefore additional reference frames for the different conditions are to be captured and evaluated. The calculated parameters including sector settings can be stored in multiple tables.

Denoise Function

The de-noise function can reduce the noise existing on edges markedly and smooth

the shades.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit.

A bad pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

Strobe Control

To achieve the plausible best image quality in low light conditions, the programmable strobe control function is integrated to control a strobe flash.

Strobe Mode

SP5408 includes 5 different strobe modes:

- Xeon Mode
- Led1 Mode
- Led2 Mode
- Led3 Mode
- Programmable Strobe Level Mode

Xenon Mode

In strobe mode, the number 3 frame gets strobe plus signal, when signal strobe_request get high level. The with of the plus can be programmed, from one-row-time to four-row-time. The number 3 frame can be exposed correctly. The relative timing diagram is shown below.

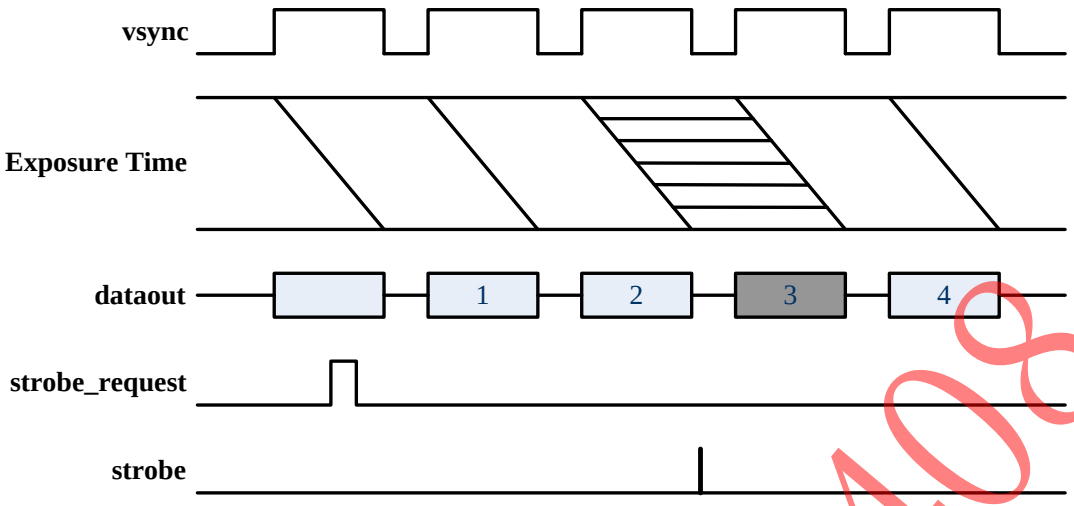


Figure 5 Xenon Mode

Register for Xenon Mode:
0xfd = 0x01
0xb5 = 0x91
0xb5 = 0x11

LED1

When signal strobe_request is short plus, which means the time of the plus is less than two-frame-time, the strobe mode goes into LED1 mode. The number 3 frame gets strobe plus, when signal strobe_request get high level.

The time of strobe plus can be programmed by register 0xb3 and 0xb4. From number 3 frame, exposure time equals to minimum frame time plus strobe plus time.

Further more the strobe plus can output again after a few frame by setting register 0xb6. For example, when 0xb6 set 2, and the signal strobe_request gets high level, the number 3 and number 4 frame is skipped, and the number 5 frame get strobe plus, and number 6 frame gets the normal exposure time. The relative timing diagram is shown below.

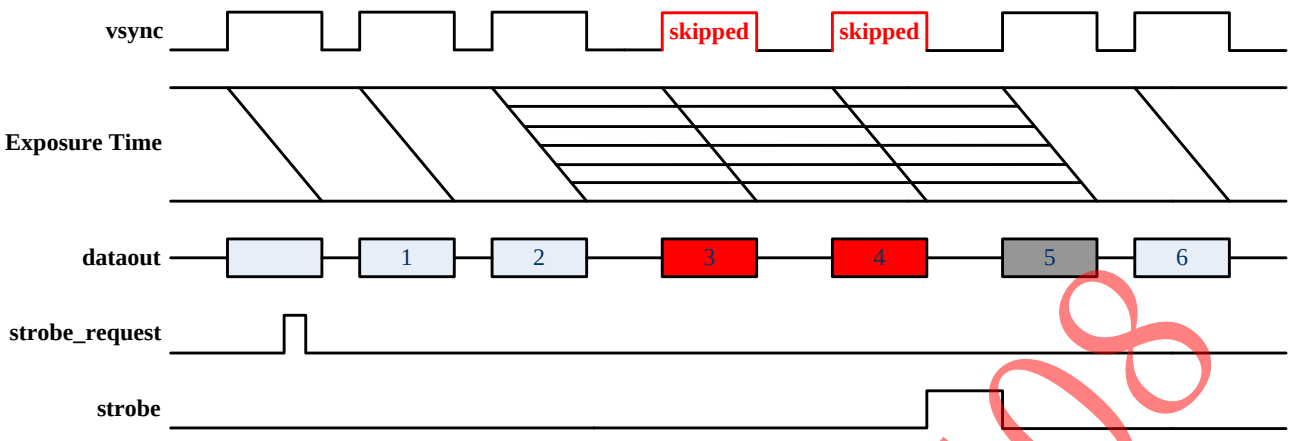


Figure 6 LED1 Mode

Register for LED1 Mode:
0xfd = 0x01
0xb3 = 0x00
0xb4 = 0x20
0xb5 = 0x82
0xb5 = 0x02
0xb6 = 0x02
0x01 = 0x01

LED2

When signal strobe_request is long plus, which means the time of the plus can cover the number 3 frame when the signal strobe_request get high level, the strobe mode goes into LED2 mode.

The number 3 frame gets strobe plus, when signal strobe_request get high level. As long as the signal strobe_request is at high level, the strobe plus keeps outputting. The time of strobe plus can be programmed by register 0xb3 and 0xb4. From number 3 frame, exposure time equals to minimum frame time plus strobe plus time.

Further more the strobe plus can output again after a few frame by setting register 0xb6. For example, when 0xb6 set 1 and signal strobe_request gets high level, the number 4 frame get strobe plus, and as long as the signal strobe_request stays at high level, the strobe plus output every 2 frame. The relative timing diagram is shown

below.

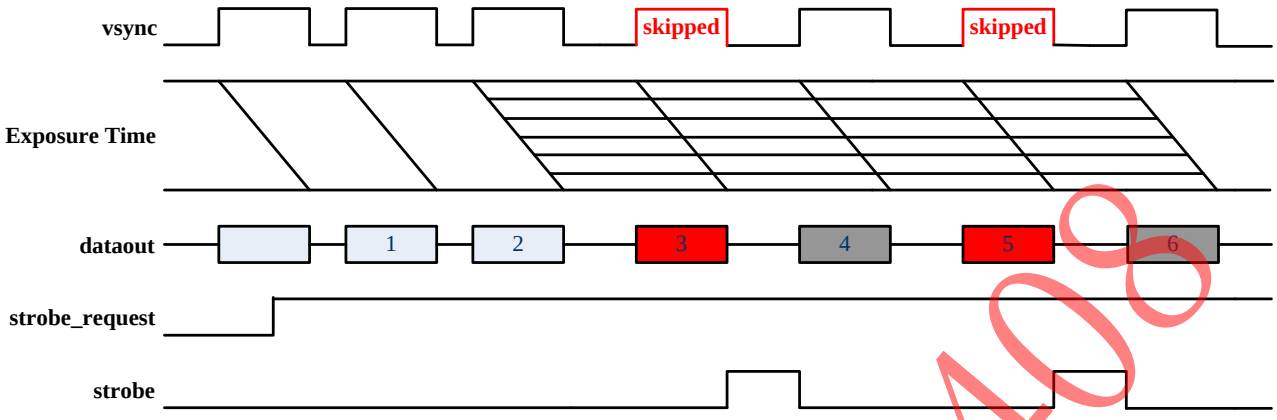


Figure 7 LED2 Mode

Register for LED2 Mode:

0xfd = 0x01

0xb3 = 0x00

0xb4 = 0x20

0xb5 = 0x82

0xb6 = 0x01

0x01 = 0x01

After several frames:

0xb5 = 0x00

LED3

When signal strobe_request is long plus, which means the time of the plus is not less than one-frame-time, the strobe mode goes into LED3 mode. Signal strobe gets high level at the next frame when the signal strobe_request gets high level, and vice versa. The relative timing diagram is shown below.

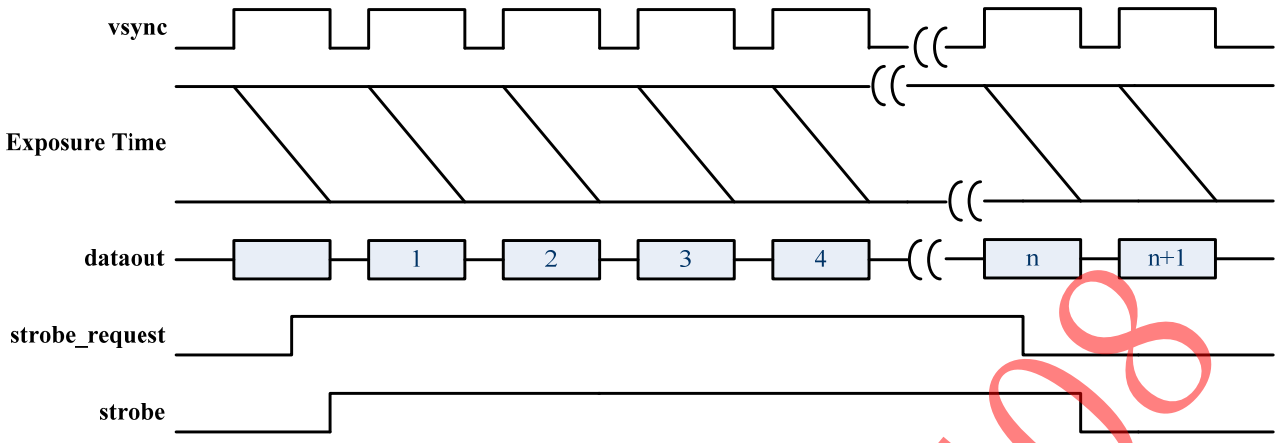


Figure 8 LED3 Mode

Register for LED3 Mode:
0xfd = 0x01
0xb5 = 0x84
After several frames:
0xb5 = 0x00

Programmable Strobe Level Mode

At programmable strobe level mode, the signal strobe output level is fixed, and can be programmed by register oxb7.

Register for Programmable Strobe Level Mode:
0xfd = 0x01
0xb5 = 0x08
0xb7 = 0x01

Output Interface

- MIPI Serial Interface

MIPI Serial Interface

MIPI Serial Interface – Mobile Industry Processor Interface is the most important

data transport path for the next generation mobile phone, which defines standards for the interface between SP5408 modules of a mobile. The MIPI interface can support large data stream better than any other data interface. With it the sensor can provide more high definition images to the mobile phone. More over, the MIPI interface enables rapid data transfer, increasing reliability, reducing power consumption and also eliminating facility compatibility issues.

MIPI interface provides one single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Data lane has full support for HS (uni-directional) and LP (bi-directional) data transfer mode.

PLL and Clock Generator

The sensor contains a Phase Locked Loop (PLL) block, which generates all the necessary internal clocks from the external clock input.

The internal function blocks of the PLL is shown below.

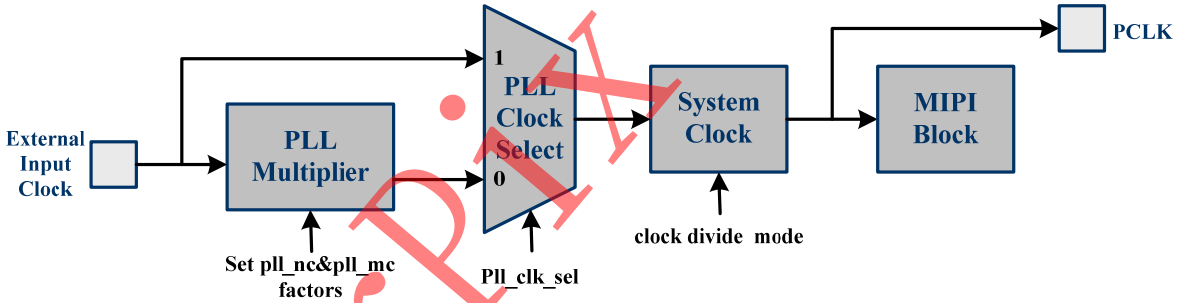


Figure 9 PLL Function Block

Address	Register Name	Bits	Description	Default
P0:0x10	clk_mode	6~0	[6]pll_clk_sel 1: system clk select external input clk 0: system clk select pll_clk [5:2]pll_nc [1:0]pll_mc pll_clk=external_clk*(pll_nc+1)/(pll_mc+1)	0x0c
P0:0x11	pclk_hsync_en, timer_clk_ctrl isp_clk_ctrl, pclk_ctrl	5~0	[5]pclk_hsync_en 1 pclk = hsync & pclk_pre 0 pclk = pclk_pre [4] timer_clk_ctrl [3:2]isp_clk_ctrl	0x00

			000: isp_clk divide 1 001: isp_clk divide 2 010: isp_clk divide 4 011: isp_clk divide 8 111: isp_clk divide 16 101: isp_clk divide 32 110: isp_clk divide 64 [1:0]pclk_ctrl	

I²C Bus

Single READ and Single WRITE

The SP5408 I²C write address and read address can be programmed by using register P0:0x00, and the default value of this register is 0x6c.

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

The figure shown below will illustrate SP5408 single READ sequence and single

WRITE sequence.

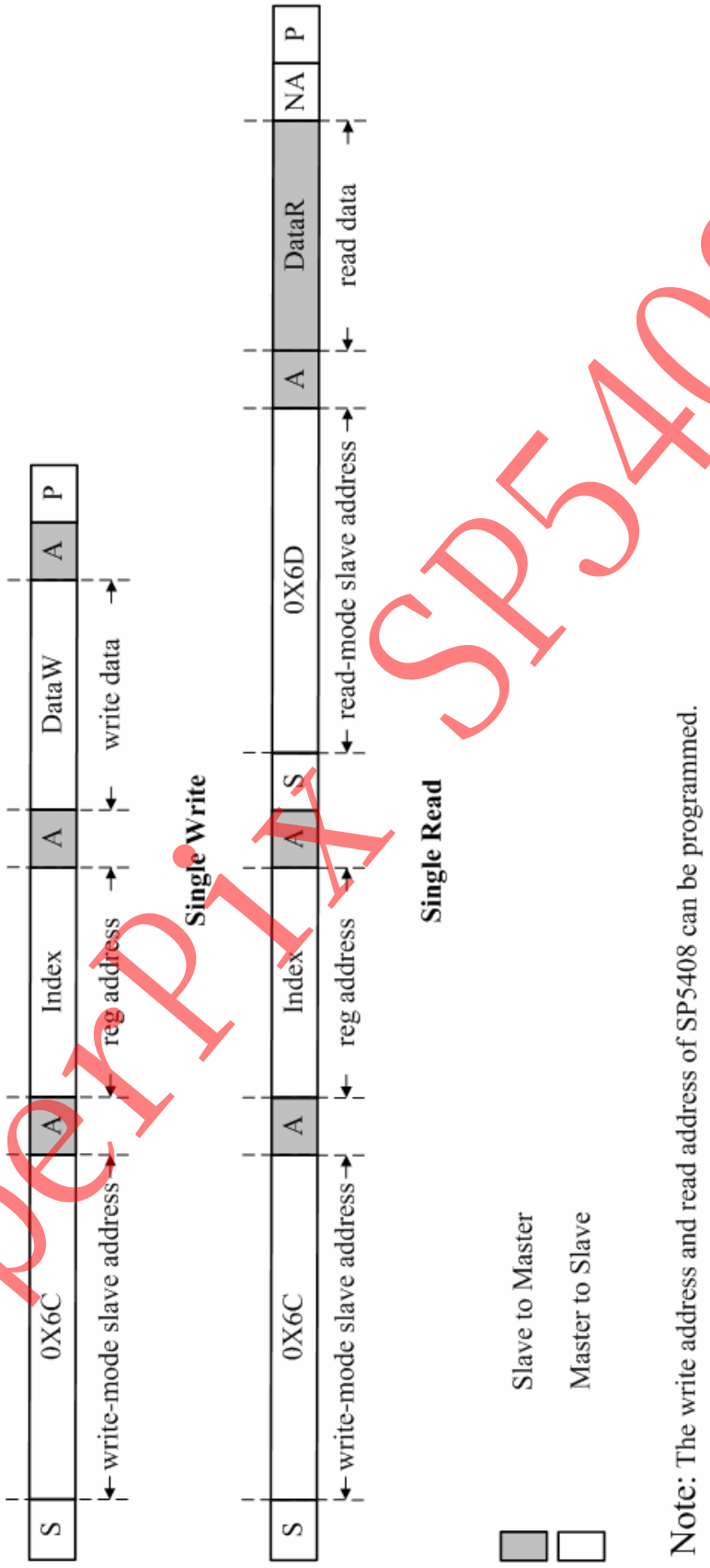


Figure 10 I²C Read & Write Message Description

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP5408 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

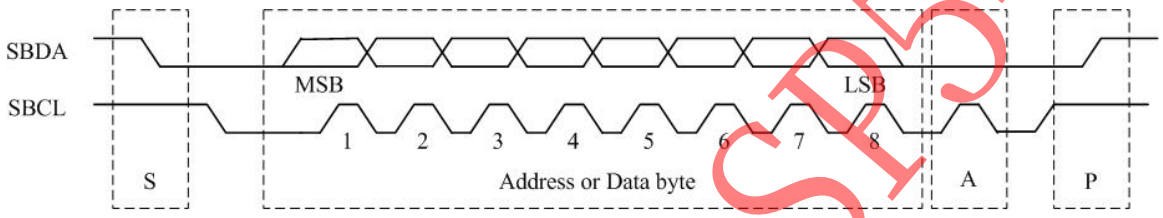


Figure 11 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

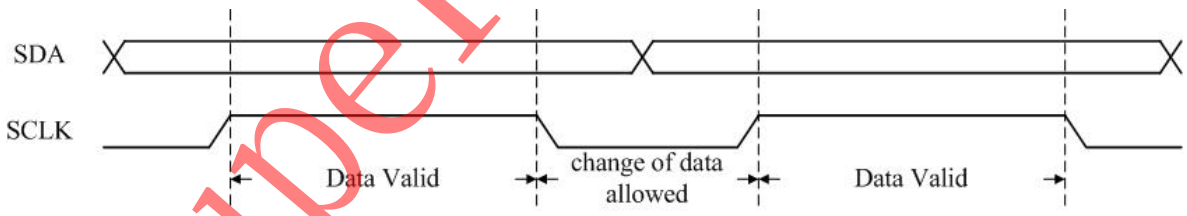


Figure 12 I²C Data Transport Description

Timing Parameter

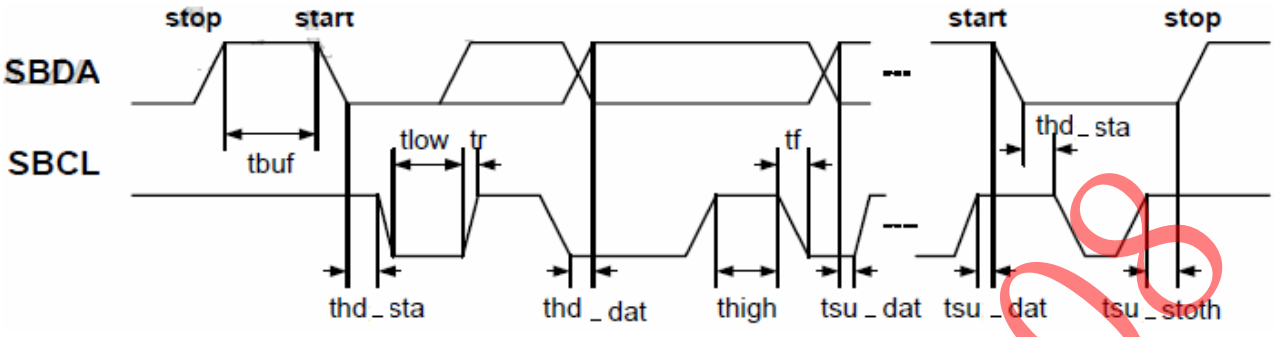


Figure 13 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

DC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.6	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		0.3xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			0.3xVDDIO	V
T	Junction Temperature	-20	25	70	**°C**

Power Up/Off Sequence

Power Up Sequence

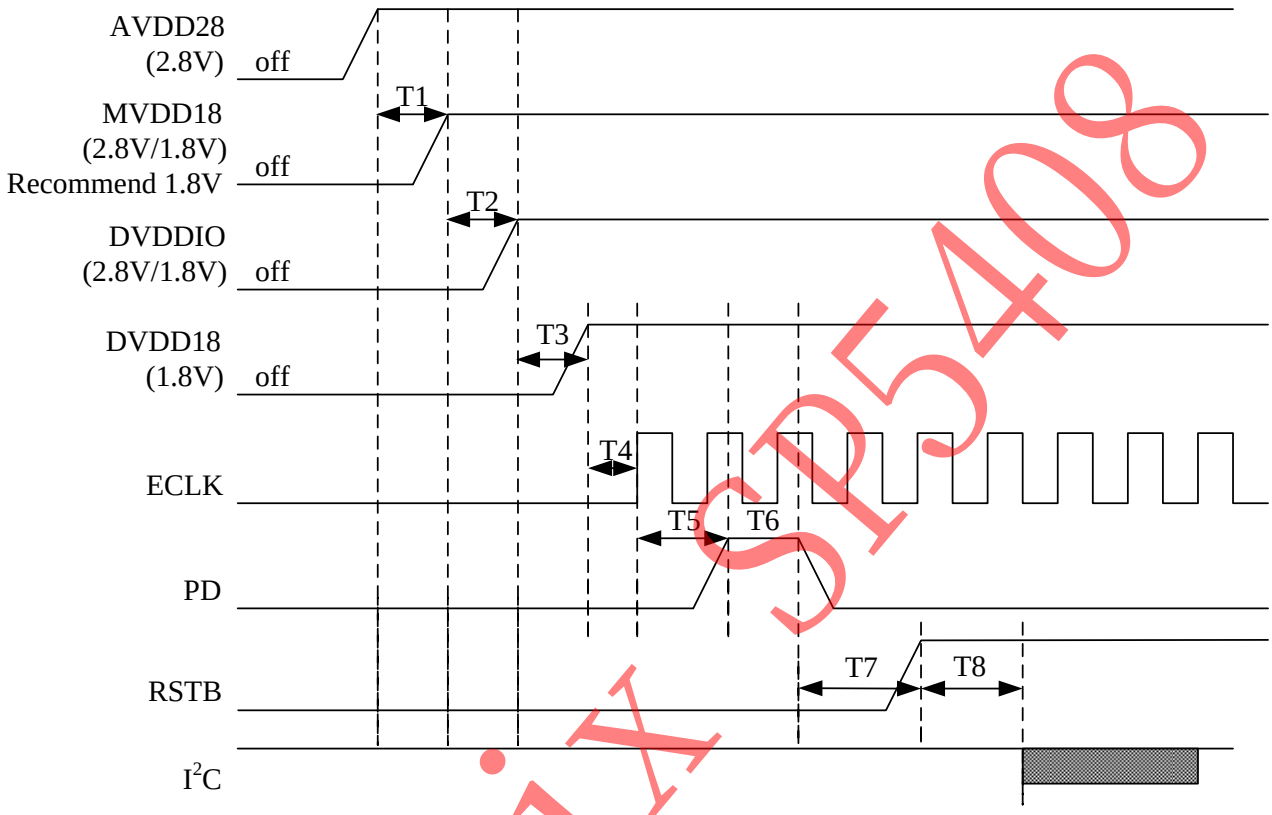


Figure 14 Power Up Sequence

Symbol	Description	Min	Unit
T1	Time from AVDD28 to MVDD28	0	ms
T2	Time from MVDD28 to DVDDIO	0	ms
T3	Time from DVDDIO to DVDD18	0	ms
T4	Time from DVDD18 to clock plus input	0	ms
T5	Time from ECLK to PD up edge	0	ms
T6	PD high plus time	100	ns
T7	Time from PD down edge to RSTB up edge	0	ms
T8	Time from RSTB up edge to available I^2C	5	ms

Note: The SP5408 sensor includes a RSTB pin that forces a complete hardware reset when it is pulled low(GND). The SP5408 sensor also includes POR circuit which generate reset signal when power up. POR generates the reset signal only occurs at power up, but RSTB generates the reset signal at anytime. If necessary, the SP5408 could used the RSTB to generate the hardware reset that following above timing. If not, the RSTB should be connected with DVDDIO.

Power Off Sequence

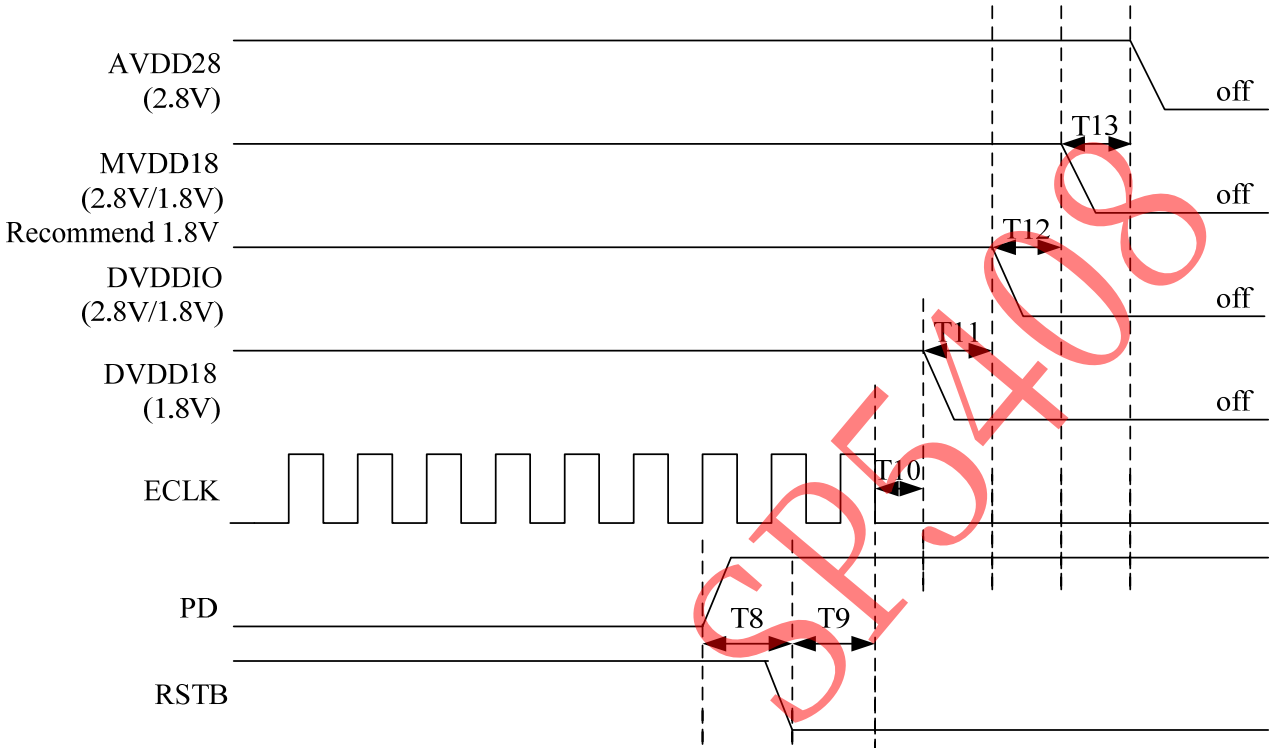


Figure 15 Power Off Sequence

Symbol	Description	Min	Unit
T8	Time from PD up edge to RSTB down edge	0	ms
T9	Time from RSTB down edge to ECLK	0	ms
T10	Time from ECLK to DVDD18	0	ms
T11	Time from DVDD18 to DVDDIO power down	0	ms
T12	Time from DVDDIO to MVDD28 power down	0	ms
T13	Time from MVDD28 to AVDD28 power down	0	ms

Note: If necessary, the SP5408 could used the RSTB to generate the hardware reset that following above timing. If not, the RSTB should be connect DVDDIO.

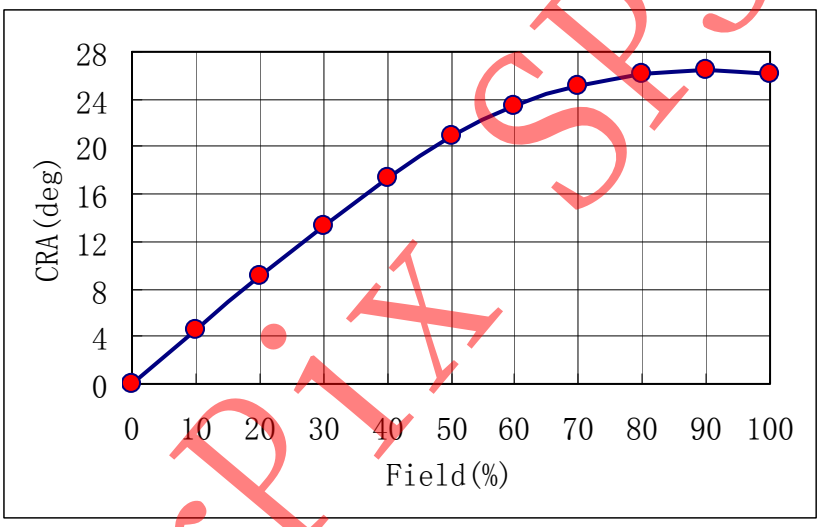
CRA Information

Pixel Array Information

Unit Pixel Size: 1.4um

		Value
Active pixel array	X-axis	2592
	Y-axis	1944
RIC(mm)	X-axis edge	1.814
	Y-axis edge	1.361
	Diagonal edge	2.268

RIC: Radius from the Image Center

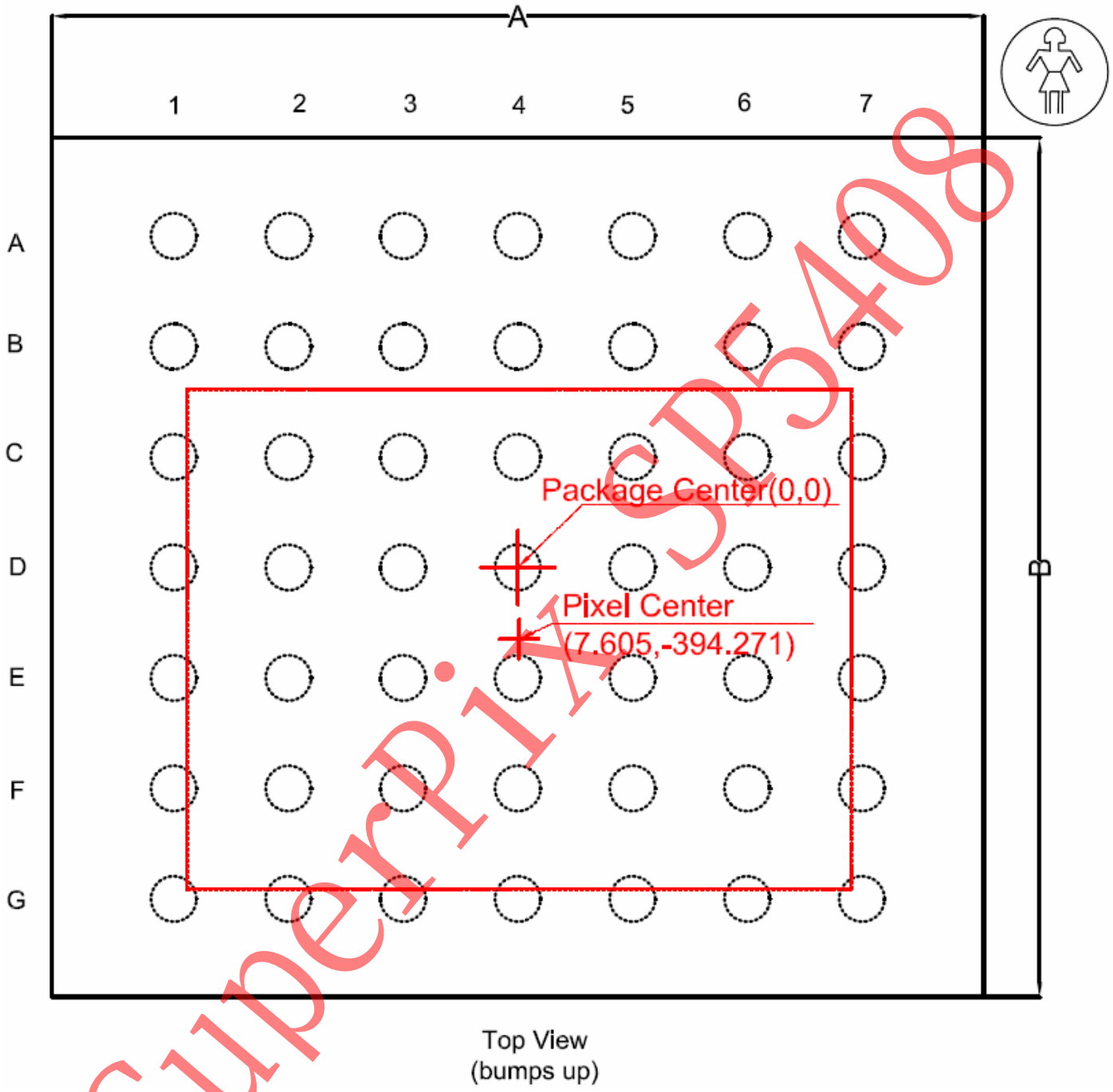


Field(%)	RIC(mm)	CRA(deg)
0	0	0
10	0.2268	4.6
20	0.4536	9.1
30	0.6804	13.4
40	0.9072	17.4
50	1.134	20.9
60	1.3608	23.4
70	1.5876	25.1
80	1.8144	26.2
90	2.0412	26.4
100	2.268	26.1

Figure 16 CRA Information

Package Information

Unit: um



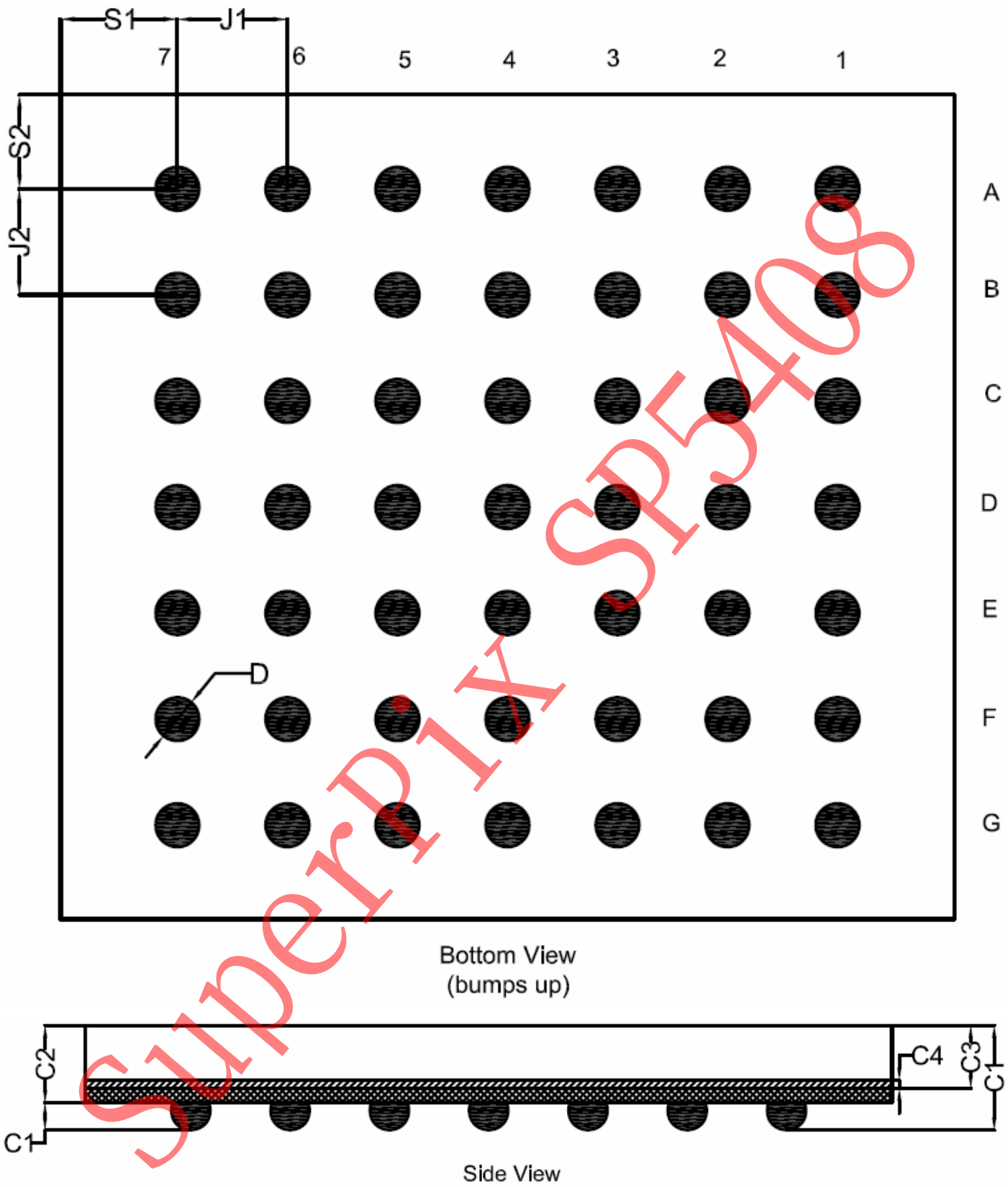


Figure 17 Package Information

	1	2	3	4	5	6	7
A	RSTB	PWDN	DVDD15	DVDD18	D2	DVDD28	D8
B	SBCL	STROBE	DGND	D0	D1	D5	ECLK
C	DVDD28	BYPASS_LDO	VSYNC	HSYNC	D3	D6	D9
D	PCLK	DVDD15	SBDA	DGND	D4	D7	DGND
E	D0M	D0P	DCP	AGND28	DVDD15	DGND	DVDD28
F	D1M	D1P	DCM	AGND28	AVDD28	AVDD28	AVDD28
G	MVDD28	MVDD15	MGND28	AGND28	AVDD28	AVDD28	AGND28

Figure 18 Ball Position

Table1 Package Dimensions	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	5118	5098	5138
Package Body Dimension Y	B	4718	4698	4738
Package Height	C	667	633	701
Glue(between cover grass and sensor)	C4	50	45	55
Thickness of glass surface to wafer	C3	400	385	415
Package Body Thickness	C2	493	466	520
Ball Height	C1	174	154	194
Ball Diameter	D	250	240	260
Total Ball count	N	49	---	---
Pin pitch1 X axis	J1	630	---	---
Pin pitch Y axis	J2	607	---	---
Edge to Pin Center Distance along X	S1	669	639	699
Edge to Pin Center Distance along Y	S2	538	508	568

Figure 19 Package Dimension

NO.	PAD Name	I/O	Description
A1	RSTB	I	Reset Signal,Low level reset
A2	PD	I	Power down,"0" normal
A3	DVDD15	DP	While "BYPASS_LDO" Pin connect to"0",internal power supply 1.5V. While "BYPASS_LDO" Pin connect to"1",external power supply 1.5V.
A4	DVDD18	DP	Digital Power 1.8V
A5	D2	O	Pixel Array Output bit 2
A6	DVDD28	DP	Digital Power 2.8V
A7	D8	O	Pixel Array Output bit 8
B1	SBCL	I	Slave I2C clock bus
B2	STROBE	O	Strobe Signal
B3	DGND	DG	Digital Ground
B4	D0	O	Pixel Array Output bit 0
B5	D1	O	Pixel Array Output bit 1
B6	D5	O	Pixel Array Output bit 5

B7	ECLK	I	Input system clock
C1	DVDD28	DP	Digital Power 2.8V
C2	BYPASS_LDO	O	"0"Internal Power supply,"1"External Power supply.
C3	VSYNC	O	Vertical Sync Signal
C4	HSYNC	O	Horizontal Sync Signal
C5	D3	O	Pixel Array Output bit 3
C6	D6	O	Pixel Array Output bit 6
C7	D9	O	Pixel Array Output bit 9
D1	PCLK	O	Pixel Output Clock
D2	DVDD15	DP	The same as PAD"A3" description
D3	SBDA	I/O	Slave Tri-state,I2C data bus
D4	DGND	DG	Digital Ground
D5	D4	O	Pixel Array Output bit 4
D6	D7	O	Pixel Array Output bit 7
D7	DGND	DG	Digital Ground
E1	D0M	O	MIPI Data0 Output -
E2	D0P	O	MIPI Data0 Output +
E3	DCP	O	MIPI Clock Output +
E4	AGND	AG	Analog Ground
E5	DVDD15	DP	The same as PAD"A3" description
E6	DGND	DG	Digital Ground
E7	DVDD28	DP	Digital Power 2.8V
F1	D1M	O	MIPI Data1 Output -
F2	D1P	O	MIPI Data1 Output +
F3	DCM	O	MIPI Clock Output -
F4	AGND	AG	Analog Ground
F5	AVDD	AP	Analog Power 2.8V
F6	AVDD	AP	Analog Power 2.8V
F7	AVDD	AP	Analog Power 2.8V
G1	MVDD28	MP	MIPI Power 1.8V
G2	MVDD15	MP	External Connect capacitance(1uF)
G3	MGND28	MG	MIPI Ground
G4	AGND	AG	Analog Ground
G5	AVDD	AP	Analog Power 2.8V
G6	AVDD	AP	Analog Power 2.8V
G7	AGND	AG	Analog Ground

Table 2 Pin Description

Revision History

Version #	Date	Modification
Commercial 1.0	2013.01.14	1. The first release for customers
Commercial 1.1	2013.06.26	1. edit key performance parameters 2. edit description in the second cover page 3. edit register description in PLL and Clock Generator 4. edit CRA information 5. add Power up/off sequence 6. ad d pixel array structure 7. edit TSV package information