1/5 Inch 2 Mega CMOS Image Sensor
SP2518

Specification

Version Commercial 2.6

2012.11.27

SuperPix Micro Technology Co., Ltd

1/5 Inch 2 Mega CMOS Image Sensor Part Number SP2518

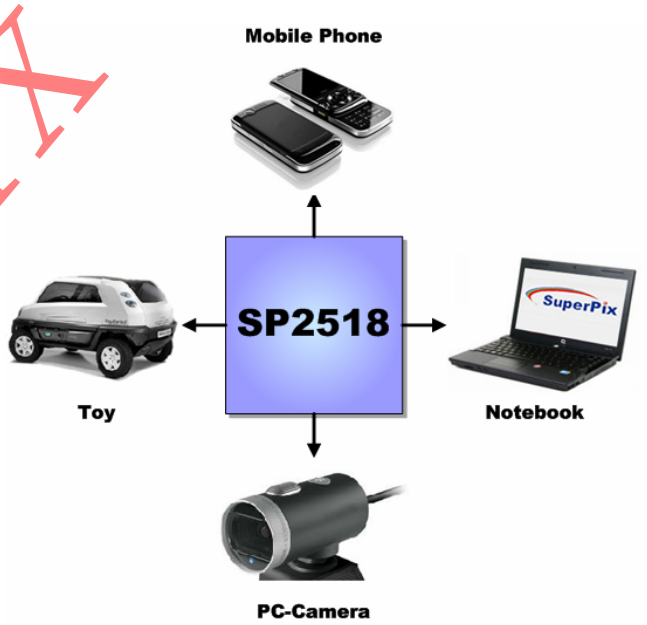
SuperPix® SP2518 is a 1/5 inch 2 Mega color digital image sensor based on the 2nd generation CMOS image sensor technology and the latest 1.75um pixel architecture stem from SuperPix® proprietary design. A plenty of sophisticated functionalities and refined image signal processors are embedded in SP2518, and make it an ideal choice for build-in camera of handset equipment, for instance, mobile phone, tablet, laptop and web camera. The prominent preprocessing functions can deliver extraordinary images to users, and in the meantime the chip consumes a very low power compared with other chips having the same resolution. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products. When it works with SuperPix® SP0827, they can provide high cost performance dual sensor solution.

Functionalities

- CMOS Image Sensor
- Image Signal Processor

Applications

- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys



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Overview

General Description

SuperPix® SP2518 is a 1/5 inch 2 Mega color digital image sensor based on the 2nd generation CMOS image sensor technology and the latest 1.75um pixel architecture stem from SuperPix® proprietary design. A plenty of sophisticated functionalities and refined image signal processors are embedded in SP2518, and make it an ideal choice for build-in camera of handset equipment, for instance, mobile phone, tablet, laptop and web camera. The prominent preprocessing functions can deliver extraordinary images to users, and in the meantime the chip consumes a very low power compared with other chips having the same resolution. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products. When it works with SuperPix® SP0827, they can provide high cost performance dual sensor solution.

A high performance system on a chip (SOC) sensor, SP2518 is a chip built on SuperPix® proprietary pixel and ISP technology for the users who demand high quality sensor for multiple realms. SP2518's image signal processor includes automatic exposure control, gain control, white balance, black level calibration, lens correction, defect pixel canceling and more. Additionally, it also features all standard image quality controls such as color saturation, hue, gamma, sharpness (edge enhancement) and noise cancellation. Camera controls are accessed over a standard serial camera control bus interface. Other key image processing features minimize spatial artifacts and removes image artifacts around edges to deliver clean, crystalline images, critical for achieving best-in-class 2-megapixel images.

Extending the company's portfolio of 2-megapixel sensor, the 1.75um pixel architecture enables the SP2518 to offer high performance imaging and high definition video in an ultra-compact 1/5 inch optical format, making it an ideal choice for mainstream handset equipments. The advanced pixel architecture delivers excellent low-light performance for the next generation of high performance mobile phones or PCs.

SP2518 operates at high frame rates, offering 720P resolution at 30 frames per second (fps), and UXGA resolution at 15 frames per second (fps). SP2518 comes with a standard serial I^2C interface and a high speed parallel output interface delivering RAW or YUV or RGB image data.

An overview of the SP2518 Image Sensor features and functions will be given below.

Function Diagram

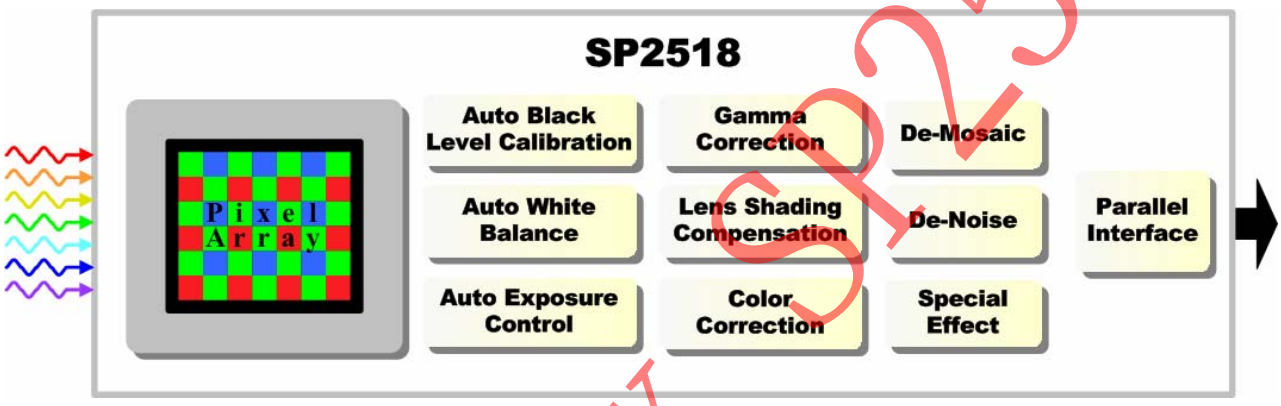


Figure 1 Function Diagram

Typical Application List

- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys

Typical Application Diagram

Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	1600 x 1200
Pixel Size	1.75um x 1.75um Square Pixel
Lens Size	1/5 inch
Color Filter	Primary Color Filter Bayer arrangement
Power Supply	I/O 1.7V ~ 3.0V
	Analog 2.6V ~ 3.0V
Power Consumption	Active < 100mA
	Standby 75uA
Data Formats	Raw Bayer 8bit / 10bit
	YUV422
	RGB565
Output Format	8bit Parallel
Input Clock	6 – 30 MHz
Max. Frame Rate	15fps@1600 x 1200 Mode
	30fps@1280 x 720 Mode
	50fps@ 800 x 600 Mode
	50fps@ 640 x 480 Mode
Shutter	Rolling shutter
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	COB / TSV

Table 1 Key Performance Parameters

Features List

- Support UXGA (1600x1200), 720P (1280x720), and VGA (640x480) resolution
- Embedded image preprocessor functionality
  - Automatic Black Level Calibration
  - Automatic White Balance
  - Automatic Exposure Control
  - Gamma Correction
  - Lens Shading Compensation
  - De-mosaic Function
  - De-noise Function
  - Color Correction Function
  - Special Effect: monochrome, negative, sepia, sketch, and emboss
- Support I²C bus controlling registers inside chip
- Support strobe signal in order to control flash lamp
- Support single or multi-group power supply
- Support SPI data input
- Support a host of mobile phone platform
- Compatible with QVGA or VGA sensor chip for low-cost Dual-Sensor solution

Function Description

Pixel Array Structure

The SP2518 pixel array is configured as of 1608 columns by 1216 rows, shown below. There are 1600 columns by 1200 rows of optically active pixels. The active area is surrounded with optically transparent dummy 24 columns and 24 rows to improve image uniformity with in the active area.

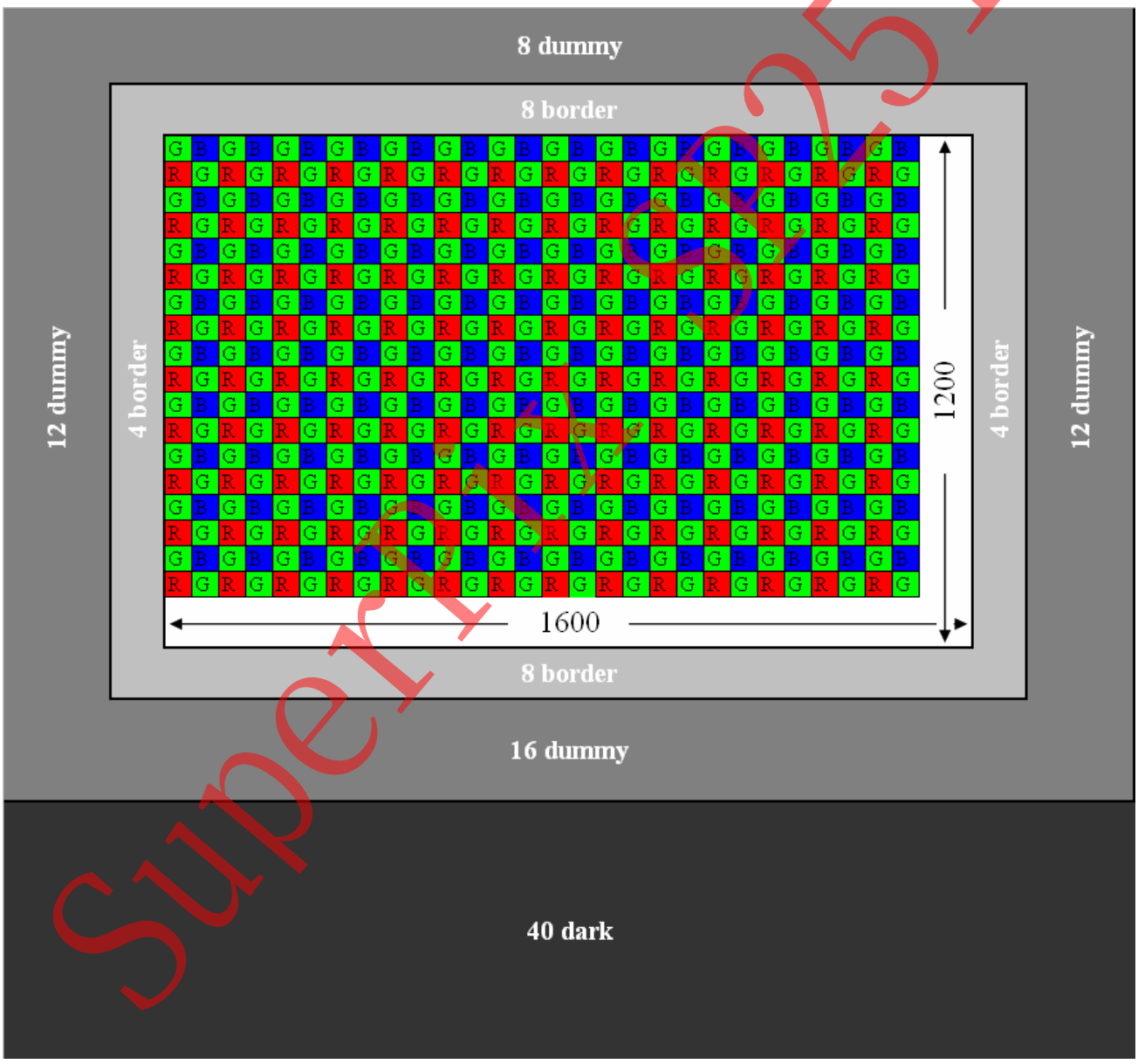


Figure 3 Pixel Array Structure Detail

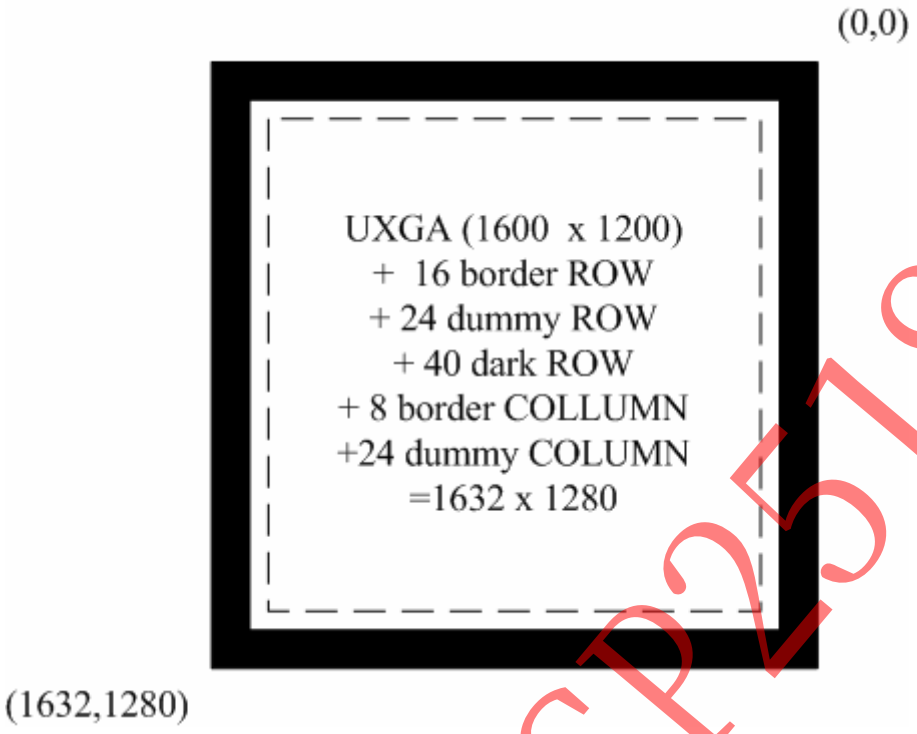


Figure 4 Sensor Pixel Description

Image Sensor Function

- Mirror and Flip
- Windowing
- Test Pattern
- Automatic Black Level Calibration
- Automatic White Balance
- Automatic Exposure Control
- Automatic Black Level Correction
- Gamma Correction
- Lens Shading Compensation
- De-mosaic Function
- De-noise Function
- Color Correction Function
- Bad Pixel Correction
- RGB to YUV Conversion
- YUV to RGB Conversion
- Special Effect
- Parallel Interface

Mirror and Flip

Mirror and Flip read out modes are provided, and can reverse the sensor data read out order horizontally and vertically respectively.

Original Mirrored Flipped Mirrored and Flipped

Figure 5 Mirror and Flip

Windowing

The embedded windowing function extract an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By property setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

Test Pattern

Test pattern, color bar, is offered for testing purpose.

Automatic Black Level Calibration

The pixel array contains several optically black lines, which can be seen at the pixel array structure section. These lines are used to provide the data for black level calibration and further correction.

Automatic White Balance

Auto white balance unit is help to remove the unrealistic color from the image automatically by referencing the white balance pre-gain. With auto white balance unit, the still / video camera system can determine the color temperature of the light and automatically adjust for the color temperature.

Automatic Exposure Control

After Gamma unit, the Y value, calculated by R, G, and B values, used to evaluate the luminance and exposure time, digital gain, analog gain are adjusted by this block to get the right luminance for the image.

Gamma Correction

The main purposed of the Gamma correction function is to compensate the characteristics of the sensor. According to de gamma curve, the pixel values can be converted in order to compensate the sensor output on different light strength conditions.

Lens Shading Compensation

Lens imperfection can be eliminated by lens shading compensation. It starts with the first pixel of a frame when the lens shading compensation unit is enabled, and correcting each pixel with its gain values.

The lens shading correction is based on one or more reference frames which have to be captured under dedicated light conditions and a dedicated position of the sensor. The pixels of the captured frame are then evaluated by software and the calculated parameters for lens shading correction are stored in different tables. It is also possible to use different lens shading correction parameters for different environment conditions. Therefore additional reference frames for the different conditions are to be captured and evaluated. The calculated parameters including sector settings can be stored in multiple tables.

De-mosaic Function

De-mosaic function is to convert the raw data to RGB image data. The algorithm is a digital image process used to interpolate a complete image from the partial raw data received form the color filter in form of a matrix of colored pixels. Each raw pixel data is converted to RGB value using an edge-sensitive color interpolation algorithm.

De-noise Function

The de-noise function can reduce the noise existing on edges markedly and smooth the shades.

Color Correction Function

The color correction function is including various color profiles that are used for color representation improvement. The function works by making decision based on scene brightness and illumination type.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor pixel during the Bad Pixel Correction unit. A bad pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such bad pixels will be detected and corrected.

RGB to YUV Conversion

It is used to convert the RGB color space to YUV color space so that the following image processing can be done in the YUV color space.

YUV to RGB Conversion

This block converts YUV to RGB so that the ISP can output RGB directly.

Special Effect

A set of image special effect is supported which includes monochrome, negative, sepia, sketch, and emboss.

Strobe Control

To achieve the plausible best image quality in low light conditions, the programmable strobe control function is integrated to control a strobe flash.

Strobe Signal

The strobe signal generated by SP5408 can be programmable, and SP5408 provide 3 different modes which will be illustrated below.

Strobe Mode 0 & 1

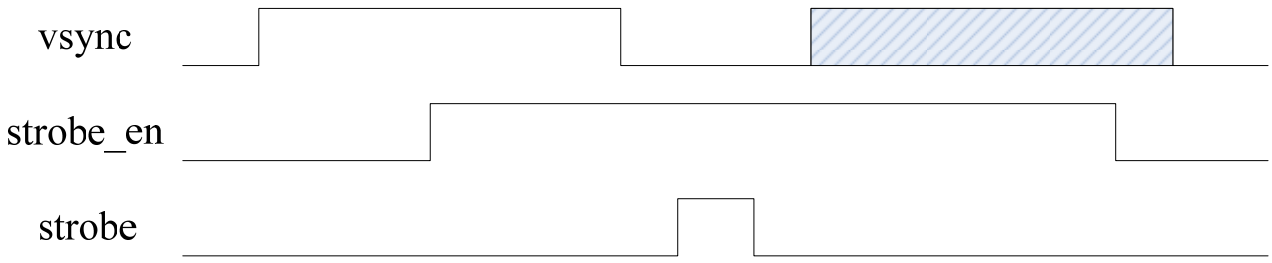


Figure 6 Strobe Mode 0 & 1

When the strobe signal is triggered in mode 0 or 1, the strobe signal will be launched at “vblank” level, the width of it can be chosen as 1 or 4, and the next frame – the one is colored shown at the figure above – then can be exposed accurately.

mode 0, 1 row width strobe
mode 1, 4 row width strobe

Strobe Mode 2

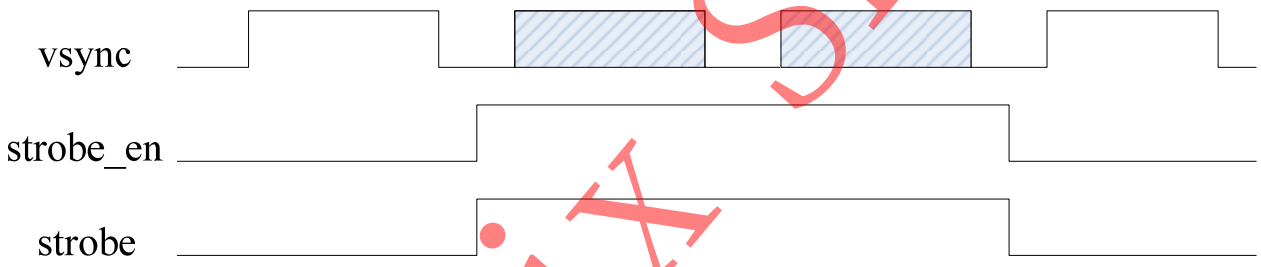


Figure 7 Strobe Mode 2

When the strobe signal is triggered in mode 2, the strobe signal will be launched immediately, and the next frame – the one is colored shown at the figure above – then can be exposed accurately.

Strobe_sel =2 : mode 2

Parallel Interface

Parallel Interface defines an interface between a peripheral device and a host processor. The parallel interface tends to be the output interface of most camera devices, and can be configured to operate as a camera interface. This sensor is built on the heritage and experience in the concept of high quality Superpix® traditional high speed parallel interface.

I²C Bus

Single READ and Single WRITE

The SP2518 I²C write address is 60H and read address is 61H. A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Tow figures that is shown below will illustrate SP2518 single READ sequence and single WRITE sequence.

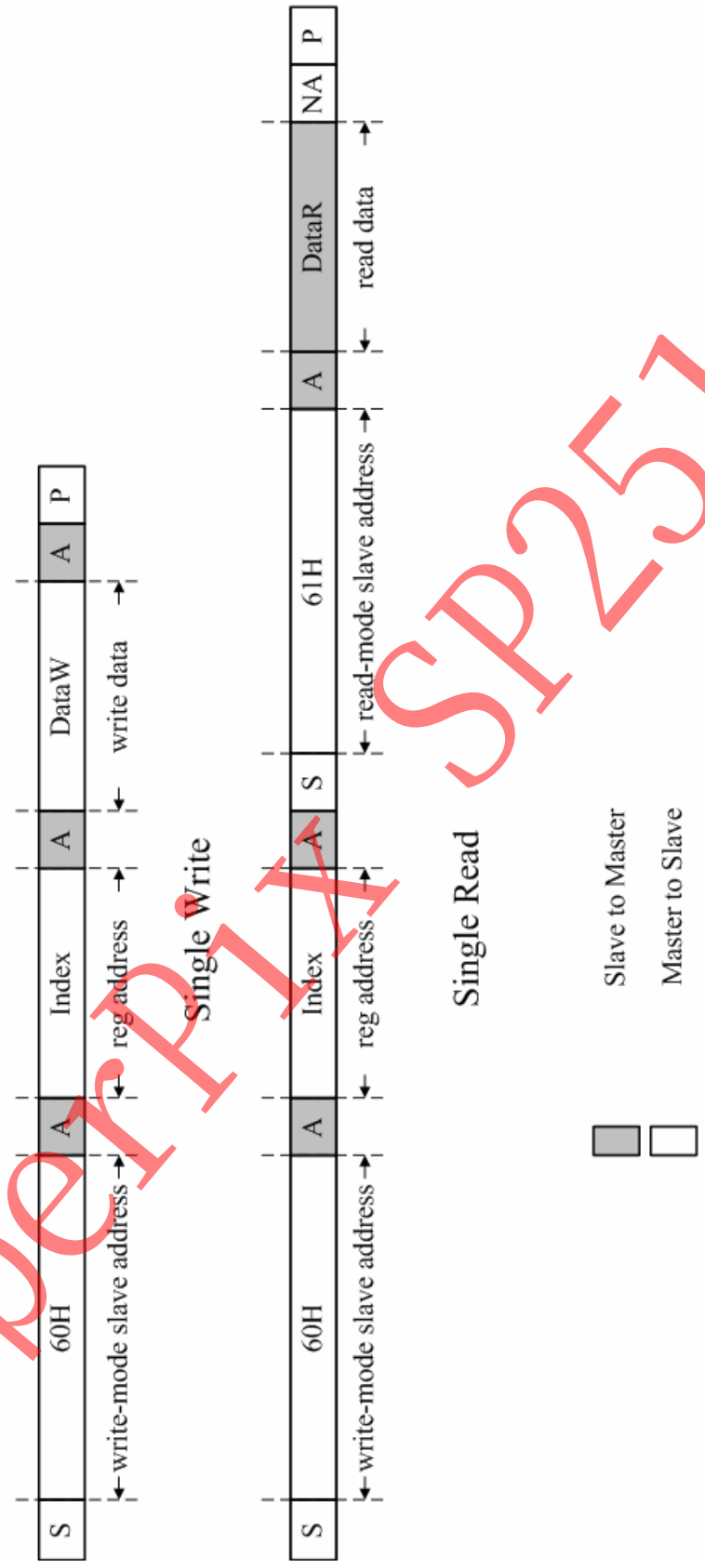


Figure 8 I²C Read & Write Description

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP0838 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

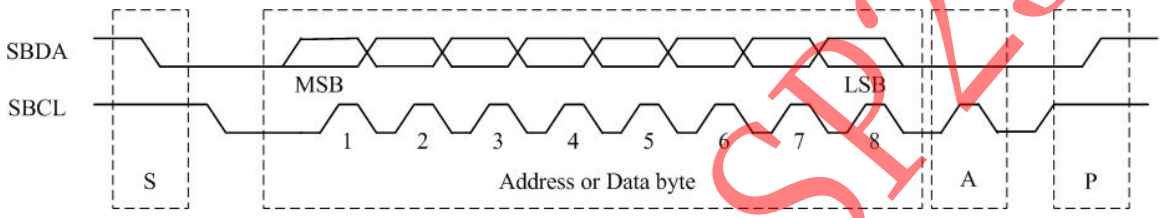


Figure 9 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

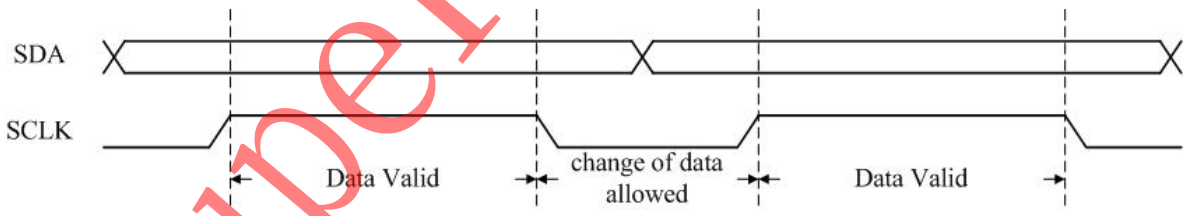


Figure 10 I²C Data Transport Description

Timing Parameter

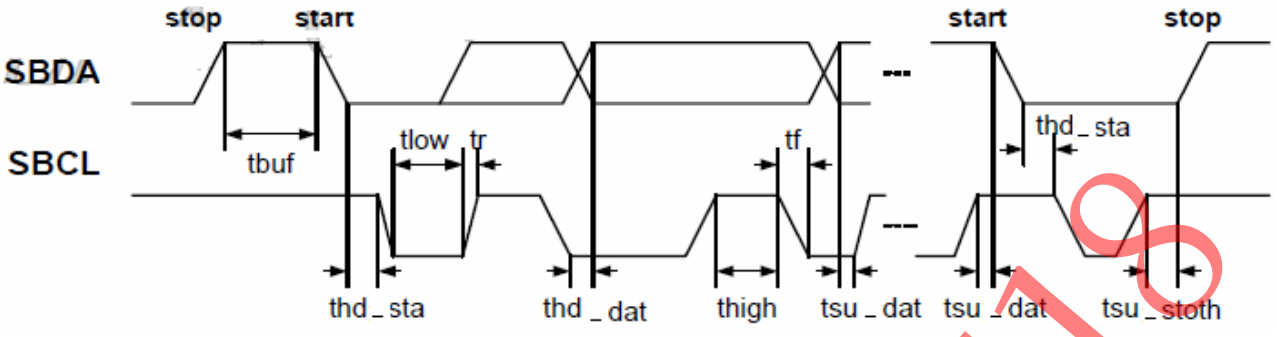


Figure 11 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	10	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

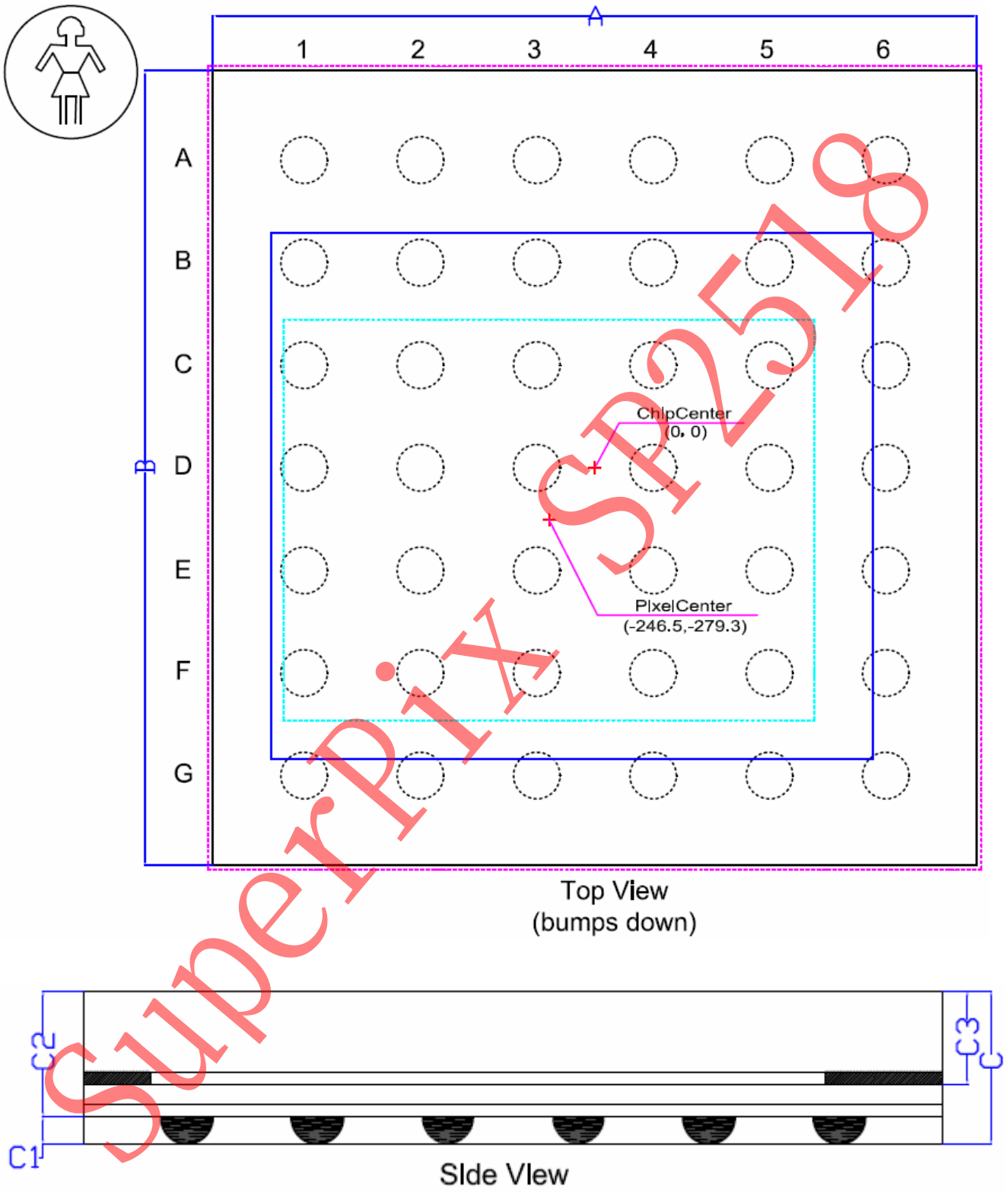
DC Specifications

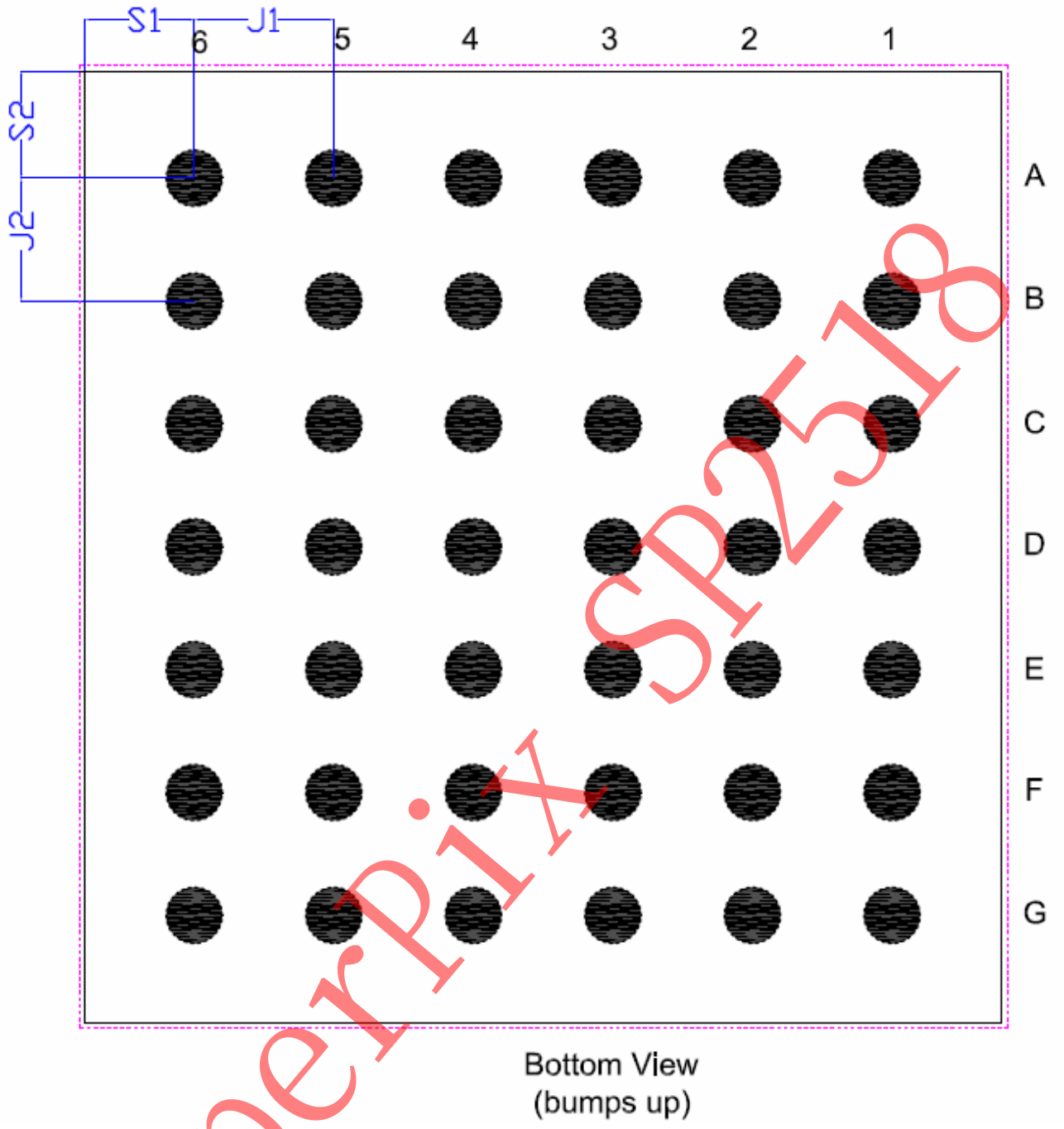
Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.6	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		0.3xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			0.3xVDDIO	V
T	Junction Temperature	-20	25	70	°C

Examination Item

No.	Reliability Items	Condition
1	Temp Cycle	-20°C ~ 70°C each 30 min, 24 cycles
2	High Temp. & Humidity storage	70°C / 80% / 72Hr
3	Low Temp. & Humidity storage	-20°C / 96Hr natural dry, for 3 hours
4	High Temp Operating	70°C / 80% / 72Hr / 2.8V other pins are active condition
5	Low Temp Operating	-20°C / 72Hr / 2.8V other pins are active condition
6	Drop Test	1.5m drop, 1 X 6 plane (Camera with 100g cradle)
7	Random Vibration	5~100HZ, 3 axis (X,Y,Z),15min/axis,swing :6mm

Package





	1	2	3	4	5	6
A	D[0]	DVDD28	DGND	PCLK	DGND	DVDD28
B	D[1]	D[2]	D[3]	D[5]	D[7]	D[9]
C	DVDD18	STROBE	D[4]	HSYNC	D[8]	CVDD28
D	DGND	DVDD15	VSYNC	D[6]	DVDD15	AGND28
E	DVDD28	ECLK	BYP_LDO	PD	AGND28	AGND28
F	SDBA	RST	SCLK	\	AGND28	AVDD28
G	AVDD28	AGND28	PVDD28	\	AGND28	AVDD28

Figure 12 Pin Name

Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	4105	4080	4130
Package Body Dimension Y	B	4259	4234	4284
Package Height	C	730	670	790
Ball Height	C1	130	100	160
Package Body Thickness	C2	600	565	635
Thickness of glass surface to wafer	C3	445	425	465
Ball Diameter	D	250	220	280
Total Ball count	N	42	–	–
pin pitch X axis	J1	625	–	–
Pin pitch Y axis	J2	550	–	–
Edge to Pin Center Distance along X	S1	490	460	520
Edge to Pin Center Distance along Y	S2	479.5	450	510

Figure 13 Package Dimensions

PIN#	PAD_NAME	I/O	Description	PIN#	PAD_NAME	I/O	Description
A1	D[0]	O	Pixel Array Output Bit 0	D4	D[6]	O	Pixel Array Output Bit 6
A2	DVDD28	DP	Digital I/O Power 2.8V	D5	DVDD15	DP	Digital core power 1.5V, internal only
A3	DGND	DG	Digital Ground				
A4	PCLK	O	Pixel Output Clock	D6	AGND28	AG	Analog Ground
A5	DGND	DG	Digital Ground	E1	DVDD28	DP	Digital I/O Power 2.8V
A6	DVDD28	DP	Digital I/O Power 2.8V	E2	ECLK	I	Input Clock
B1	D[1]	O	Pixel Array Output Bit 1	E3	BYP_LDO	I	"0"Internal Power,"1"External Power
B2	D[2]	O	Pixel Array Output Bit 2	E4	PD	I	Power Down,"0"Normal
B3	D[3]	O	Pixel Array Output Bit 3	E5	AGND28	AG	Analog Ground
B4	D[5]	O	Pixel Array Output Bit 5	E6	AGND28	AG	Analog Ground
B5	D[7]	O	Pixel Array Output Bit 7	F1	SDBA	I/O	Slave Tri-state,I2C Data Bus
B6	D[9]	O	Pixel Array Output Bit 9	F2	RST	I	Rst Signal
C1	DVDD18	DP	Digital Power 1.8V	F3	SCLK	I	Slave I2C Clock Bus
C2	STROBE	O	Strobe Signal	F4	NC		
C3	D[4]	O	Pixel Array Output Bit 4	F5	AGND28	AG	Analog Ground
C4	HSYNC	O	Horizontal Sync Signal	F6	AVDD28	AP	Analog power 2.8V
C5	D[8]	O	Pixel Array Output Bit 8	G1	AVDD28	AP	Analog power 2.8V
C6	CVDD28	CP	Charge-pump power 2.8V	G2	AGND28	AG	Analog Ground
D1	DGND	DG	Digital Ground	G3	PVDD28	PP	Pixel Power 2.8V
D2	DVDD15	DP	Digital core power 1.5V, internal only	G4	NC		
				G5	AGND28	AG	Analog Ground
D3	VSYNC	O	Verticall Sync Signal	G6	AVDD28	AP	Analog power 2.8V

Figure 14 Pin Description

Chief Ray Angle

Pixel Array Information

Unit Pixel Size: 1.75um

		Value
Active pixel array	X-axis	1600
	Y-axis	1200
RIC(mm)	X-axis edge	1.400
	Y-axis edge	1.050
	Diagonal edge	1.750

Figure 15 Pixel Array Information

RIC: Radius from the Image Center

CRA Information

Field(%)	RIC(mm)	CRA(deg)
0.00	0	0
2.86	0.05	1.11531784
8.57	0.15	3.41771104
14.29	0.25	5.76916744
20.00	0.35	8.13824704
25.71	0.45	10.49350984
31.43	0.55	12.80351584
37.14	0.65	15.03682504
42.86	0.75	17.16199744
48.57	0.85	19.14759304
54.29	0.95	20.96217184
60.00	1.05	22.57429384
65.71	1.15	23.95251904
71.43	1.25	25.06540744
77.14	1.35	25.88151904
82.86	1.45	26.36941384
88.57	1.55	26.49765184
94.29	1.65	26.23479304
100.00	1.75	25.54939744

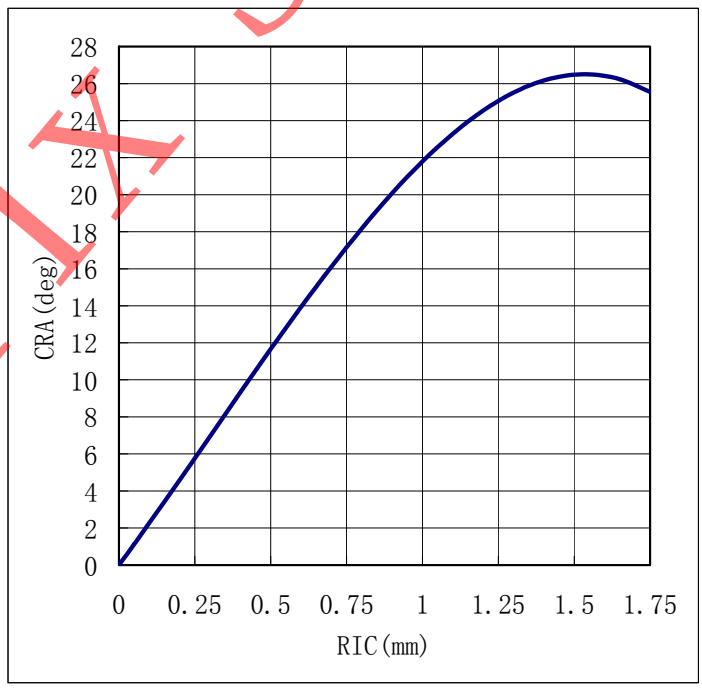


Figure 16 CRA Information

Power Up/Off Sequence

Power Up Sequence

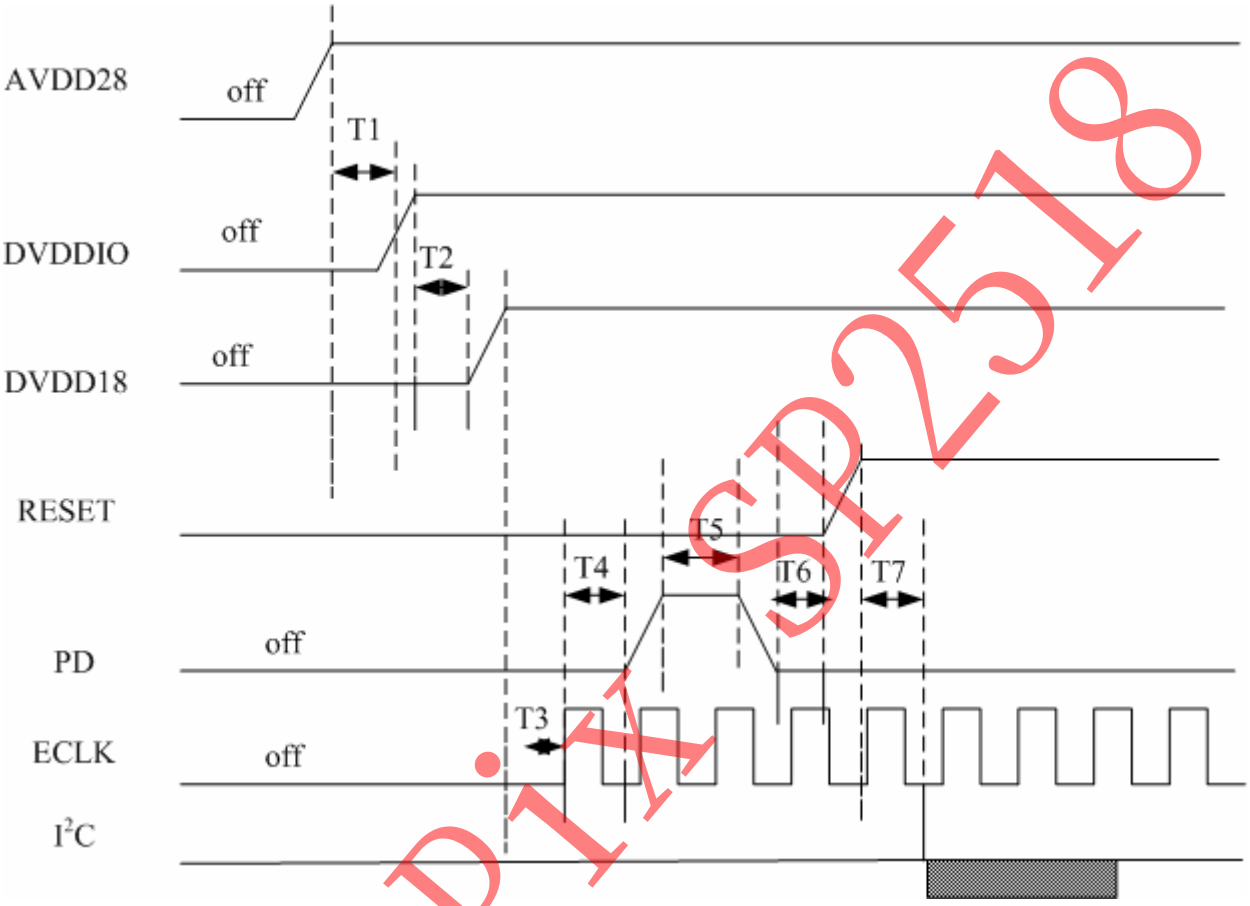


Figure 17 Power Up Sequence

Symbol	Description	Min.	Unit
T1	Time from AVDD28 to DVDDIO power up	0	ms
T2	Time from DVDDIO to DVDD18 power up	0	ms
T3	Time from DVDD18 to clock plus input	0	ms
T4	Time from clock plus input to PD up edge	0	ms
T5	PD high plus time	100	ns
T6	Time from PD down edge to RST up edge (because a POR is existent in the chip, the RESET signal should stay at high level when it power up. The RESET stay at high level when it is working stable.)	0	ms
T7	Time from PD down edge to available I^2C	5	ms

Power Off Sequence

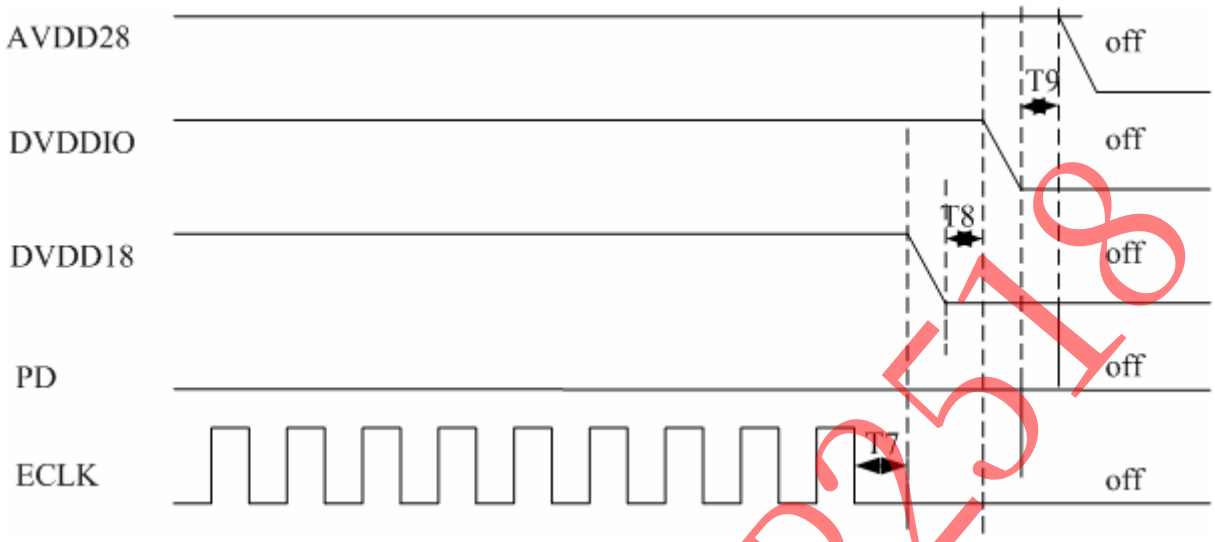


Figure 18 Power Off Sequence

Symbol	Description	Min.	Unit
T8	Time from clock plus stop to DVDD18 power down	0	ms
T9	Time DVDD18 to DVDDIO power down	0	ms
T10	Time from DVDDIO to AVDD28 power down	0	ms

Revision History

Version #	Date	Modification
Commercial 1.0	2011.10.17	1. The first version only for customers.
Commercial 1.1	2011.10.18	1. edit key performance parameters: power consumption, dark current, and SNR.
Commercial 1.2	2011.10.24	1. add package description 2. this version is only for TSV package
Commercial 1.3	2011.11.22	1. edit figure4 2. edit I^2C description
Commercial 1.4	2011.12.08	1. edit application diagram 2. add electric characteristics including DC specifications and examination item 3. edit package and pin description
Commercial 1.5	2011.12.12	1. edit table 2 package dimensions
Commercial 1.6	2012.03.23	1. edit pixel array structure
Commercial 1.7	2012.03.26	1. add Package chapter
Commercial 1.8	2012.04.16	1. edit key performance parameters: max working clock / max frame rate 2. add Chief Ray Angle 3. add Power Up/Off Squence
Commercial 1.9	2012.04.17	1. edit CRA information diagram
Commercial 2.0	2012.05.04	1. edit Key performance parameters: power consumption 2. edit the description part of pixel array structure, correct the former mistake about pixel array value
Commercial 2.1	2012.05.24	1. edit the features list 2. add strobe signal description
Commercial 2.2	2012.06.04	1. edit key performance parameters, add digital power supply
Commercial 2.3	2012.06.06	1. edit package top view, ref 12/06-06
Commercial 2.4	2012.07.05	1. edit key performance parameters 2. edit features list 3. edit I^2C timing parameter: min fscl
Commercial 2.5	2012.10.19	1. add power up/off sequence
Commercial 2.6	2012.11.27	1. update general description, key performance parameters, and features list, make them same as the latest product brief 2. update image sensor function description, add more detail description